EXPLORATION OF ENERGY- AND QOS-AWARE STRATEGIES FOR WIRED COMMUNICATION NETWORKS

by

Qun Yu

Submitted to the Graduate Faculty of

the School of Information Science

in partial fulfillment

of the requirements for the degree of

Doctor of Philosophy

University of Pittsburgh

2016

UNIVERSITY OF PITTSBURGH

SCHOOL OF INFORMATION SCIENCE

This proposal was presented

by

Qun Yu

Dr. Taieb Znati, Department of Computer Science, University of Pittsburgh

Dr. Martin B.H. Weiss, School of Information Science, University of Pittsburgh

Dr. Prashant Krishnamurthy, School of Information Science, University of Pittsburgh

Dr. Balaji Palanisamy, School of Information Science, University of Pittsburgh

Dissertation Director: Dr. Taieb Znati, Department of Computer Science, University of Pittsburgh

EXPLORATION OF ENERGY- AND QOS-AWARE STRATEGIES FOR WIRED COMMUNICATION NETWORKS

Qun Yu, PhD candidate

University of Pittsburgh, 2016

With the exponential traffic growth and the rapid expansion of communication infrastructures worldwide, energy expenditure of the Internet has become a major concern in IT-reliant society. It has motivated the urgent demands of new strategies to reduce the consumption of telecommunication networks, with particular focus on IP networks. In addition to the development of a new generation of energy-efficient network equipment, a significant body of research has focused on incorporating energy-awareness into network control and management, which aims at either reducing the network energy consumption by dynamic speed scaling of the network component to make it able to adapt its current load, or optimizing the network energy consumption through putting to sleep the redundant network elements. However, the fundamental problem of greening the Internet is to achieve a balance between the energy minimization and the demands of performance, which is an issue that received less attention but is becoming a major challenge in future network design.

In this document, I summarize my progress in the development of energy- and QoS-aware strategies for wired communication networks. Firstly, I propose and develop three families of quality-of-service (QoS)-aware packet scheduling schemes, which aim to reduce the energy consumption in network equipment by using different speed scaling strategies, while adhering to QoS requirements of supported applications. Then, I propose to further explore the problem of energy minimization under QoS constraints, through mathematical programming model, which combines speed scaling technique with an exiting scheduling policy. In addition to speed scaling approaches, I will further explore sleep-based, energy-

aware strategies, which are used to optimize energy by switching off network equipment when they are in idle state.

TABLE OF CONTENTS

1.0 INTRODUCTION

In the past few years, the Information and Communication Society (ICS) has experienced unprecedented growth in the amount of information being processed, stored, and transferred over the Internet [1]. This is due to the constantly increasing number of customers and new services being offered, as a result, data traffic volume doubles every 18 months according to Moore's law [2], which causes an even larger increase in number and capacity of network equipment to guarantee the QoS requirements of supported applications. Recent advances in semiconductor technology, which enabled higher parallelism and increased clock frequencies, paved the way to a new generation of powerful routers. These advances, however, come at a costly price of increased power consumption [3]. According to figures in 2007, Information and Communications Technology (ICT) power requirement was estimated to be within a range from 2% to 10% of global power consumption [4; 5], while energy demand of network equipment, excluding servers in data centers, was around 22 GW with expectations of reaching 95 GW in 2020 [6]. Other data related to energy consumption shows that telecom operators demand grew from 150 TWh/y in 2007 to 260 TWh/y in 2012, around 3% of the total worldwide need [7]. Finally, other work focusing on single Internet Service Provider (ISP) shows that the energy consumed by the largest ISPs, such as AT&T or China Mobile, reached 11 TWh per year in 2010, while medium sized ones like Telecom Italia and GRNET are expected to approach 400 GWh in 2015 [8].

With the dramatic increase in energy expenditures of the Internet, the power consumption of routers is becoming a bottleneck with the growing traffic, despite all of the semiconductor technology's upgrades [9; 10]. In 2009, the backbone energy consumption accounted for less than 10% of the overall network energy consumption, but this percentage is expected to increase to 40% in 2017 [9], and reach up to or even exceed 50% in 2020, and thus will become unsustainable [11; 12; 13]. In addition, another problem is that energy consumption of current IP networks is not proportional to the utilization level. So even in low or no usage context, networks equipment consumes energy at high level [1].

For these reasons, the key of future network design is to seek new strategies, incorporating energy-awareness into network control and management, to reduce power and energy consumption [14; 15; 16]. Currently, two of the most exciting dynamic power management (DPM) techniques are speed scaling and sleep mode [17]. The former is used to reduce energy consumption by dynamically adjusting clock frequencies of the active component to make it able to adapt the current load. The latter is used to save energy by putting network elements into sleep state when they are in idle state or not used. Excessive reduction in execution rates or extended sleep periods to save energy, however, could result in severe network degradation which in turn may lead to violation of QoS requirements of the underlying applications. Consequently, it becomes a significant challenge to seek effective energy-aware strategies by using these techniques to reduce energy consumption, while guaranteeing QoS performance requirements.

1.1 PROBLEM STATEMENT

The problem studied in this research is energy minimization under network QoS requirements, focusing on the exploration of energy-aware strategies to minimize the energy consumption by pursuing three aspects: (i) definition of methodologies for power- and energy-aware network design; (ii) design of energy management strategies to adapt network energy consumption to current traffic load; as well as (iii) balance achievement between saving energy and adhering to QoS performance, which is an issue that has not been well studied but is becoming a major concern in future networks.

As introduced above, two DPM techniques have been the conventionally effective methods to reduce energy consumption, which can be used to solve this problem. The speed (operations per second) of many devices can be decreased to lower the power consumption. This technique is called speed scaling, which usually results in a decreased energy consumption, despite the fact that the power is consumed for a longer time [1]. A popular speed scaling technique that is used in modern microprocessors is dynamic voltage/frequency scaling (DVFS). DVFS is applied to decrease the clock frequency (and with it, the voltage), leading to a reduced speed and power consumption. Speed scaling is also used in other devices, such as flash storage, hard drives, and network cards. Currently, various DVFS techniques [18; 19; 20; 21] are utilized to exploit the variations in actual workload for dynamically adjusting the voltage and frequency of processors, in order to achieve energy saving. Besides speed scaling, many devices support switching to a low power sleep mode to reduce the energy consumption when they are idle or not used. Typically, the challenge for DVFS techniques is to preserve the feasibility of schedule and provide performance guarantees, while the inconvenience with sleep mode techniques are that once in a power-efficient state, bringing a component back to the active or running state requires additional energy and/or delay to serve incoming traffic load, and that constantly switching network devices or their components off and on might lead to more energy consuming than keeping them on all the time. Consequently, how to use these two prominent DPM techniques to minimize network energy consumption, while adhering to QoS requirements, becomes the exploration goal of this research.

The following research questions are and to-be explored in this work:

- DVFS-based power management and QoS-aware scheduling strategies
  - How to design a DVFS-enabled, QoS-aware scheduler to minimize the energy consumption?
  - What characteristics does a QoS-aware scheduler have?
  - How to define the aggressivity for speed scaling in order to save more energy?
  - How to strike a fine balance between energy saving and network performance?
- DVFS-based power management and a load-aware, optimal energy strategy
  - What are the optimal speeds for speed scaling?
  - What characteristics the energy minimizing schedule?
  - How to well do an existing scheduling algorithm to minimize network energy consumption?

[1] Energy is power multiplied by time.

- Sleep-based power management and optimal energy strategies
  - What are the optimal sleep number for network elements?
  - How to design a sleep-based, energy-aware strategy to minimize the energy consumption?
- How to define energy efficient metrics?

1.2 RESEARCH OVERVIEW

Minimizing power and energy consumption has become a critical objective in the design of future networks. A significant body of schemes has focused on incorporating energy-awareness into network control and management. In general, they can be summarized to two categories: (i) DVFS-based techniques can reduce energy consumption by tuning the packet processing engine frequency or voltage to adapt current traffic load at different levels [18; 21; 22; 23; 24; 25; 26; 27; 28; 29]; (ii) sleep-based techniques can achieve energy saving through turning off the network devices or components when they are in idle state or not used [21; 30; 31; 32; 33; 34; 24; 25; 35; 36; 37; 38; 39]. These approaches mostly aim at managing network resources, in response to traffic load, to minimize energy and reduce congestion. However, with the advent of Internet-based multimedia communication services, such as Voice over IP (VoIP), video streaming, video conferencing, etc., QoS and Quality of Experience (QoE) become more and more important. Slowdown or shutdown a process to saving energy may lead to QoS violation. Consequently, the need to support the QoS requirements of these emerging applications further compound the energy minimization problem, calling for new energy- and QoS-aware approaches to traffic management and congestion control.

To address the above challenges and answer the aforementioned in Section 1.1, this document provides an exploration of seeking effective energy- and QoS-aware strategies based on two prominent DMP techniques, to support QoS, while achieving energy minimization.

1.2.1 DVFS-based Power Management and QoS-aware Scheduling Strategies (Completed)

The power management technique that we firstly focus on is speed scaling. Using DVFS, routers can adaptively adjust the operational frequencies of their network processor unites (NPUs), based on current conditions of the network. Excessive reduction in execution speeds to save energy, however, could result in QoS violation of the supported applications. To address the energy-QoS dichotomy, we propose and develop three families of QoS-aware packet scheduling schemes to dynamically control execution rates in network components: line cards (LCs), and reduce the energy consumption in routers. The main objective of these schemes is to minimize the dynamic energy consumed by routers through rate adaption, while achieving a balance between energy saving improvements and network performance requirements. Two metrics, namely **queue length** and **link utilization**, are considered to achieve this goal [40; 41].

1.2.2 DVFS-based Power Management and a Load-aware, Optimal Energy Strategy (in progress)

Except designing different DVFS-based, QoS-aware schedulers to reduce the evaluated energy consumption, the energy-saving issue can also be formulated by mathematical programing model. This chapter addresses a key issue of how to efficiently assign per-node delays and per-node execution speeds for a given routing path, to minimize energy consumption of network components, while satisfying the end-to-end delay requirements of the supported applications. To this end, under a given scheduling policy, we propose a DVFS-enabled, Load-aware strategy and explore several heuristics to optimize the energy consumption of network components through rate adaption, which takes into consideration the workload and the delay requirements across the routing path. In order to minimize energy consumption without violating network performance, we discuss the feasible per-node delays and the current potential processor execution speeds for a given flow, through analyzing processing capacity of delay-based processors along the path.

1.2.3 Explorations of Sleep-based Power Management (future)

This chapter involves another dynamic power management technique: sleep mode. In a network, when one network element is idle or not used, it can be put in sleep mode by shutdown it or its components, thereby achieving energy saving. In general, the base system (including chassis, switch fabric, and router processor) consumes more than half of the whole power consumption of a router. Therefore, switching off the whole router could save more energy than slowing down its components over the low-demand periods or idle periods. Considering this, our future work will further explore sleep-based, energy-aware strategies under QoS constraints, which will focus on how to achieve network energy minimization by switching off network equipment, thereby placing network resources in a more energy-efficient way.

1.3 CONTRIBUTIONS

This work makes the following contributions:

- We perform deep study on dynamic power management for wired IP networks. We propose and develop three families of QoS-aware packet scheduling schemes to minimize the network energy consumption through different speed scaling strategies, while adhering to the QoS requirements of the routed traffic.
- Targeting at energy-performance challenges, we study different metrics and try to strike a fine balance among performance, energy and accuracy. A holistic simulation framework, including an energy consumption model, is proposed to evaluate and compare the performance of each scheme, in different networking environments and traffic models.
- In order to address the energy minimization problem under a given scheduling policy, we further propose a DVFS-based, load-aware strategy through an algorithmic power management, which aims at describing a mechanism to obtain minimal energy consumption by assigning per-node delays and per-node execution speeds required across a given routing path, without network QoS violation.

- Going further, we will explore issues and challenges in sleep-based, energy-aware strategies for wired IP networks, and seek a feasible solution to minimize the energy consumption by optimizing the network configuration and putting into sleep the redundant network elements.

1.4 OUTLINE

The rest of this proposal is organized as follow: Chapter 2 briefly investigates and characterizes the sources of power consumption in wired networks, and reviews the existing dynamic power management techniques. In Chapter 3, we explore and propose three families of DVFS-based, QoS-aware scheduling schemes to minimize energy through balancing the tradeoff between the energy saving and QoS requirements. In Chapter 4, we build up a DVFS-based energy optimization framework, and further study energy minimization under a given traffic scheduling, without network QoS violation. Sleep-based power management is discussed in Chapter 5. Chapter 6 concludes the proposal and lists the timeline, respectively.

2.0 BACKGROUND

In this chapter, we firstly investigate the main sources of power consumption in wired IP networks by assessing the energy characteristics of key wire-networking components, and then introduce the existing dynamical power management techniques, aiming to review the state of the art on energy efficiency and to drive the research fostering activities toward energy- and QoS-aware solutions for future networks.

2.1 CHARACTERISTICS OF POWER CONSUMPTION IN WIRED IP NETWORKS

Routers and switches are widely used to connect different types of high-speed networks that make up the Internet today. From a general point of view, IP routers have similar architecture with respect to high-end switching systems, i.e. highly modular and hierarchical architectures [1]. A router or a switch chassis consists of three major subsystems: namely data plane, control plane and environmental units [42].

- The data plan, or called the forwarding plan, is responsible for deciding how to handle the ingress packets by looking up the routing table and then sending them to the appropriate egress interfaces (or ports). Line-cards and switch fabric cards comprise key data plane elements. The line-card is used for processing and forwarding packets using its local processing subsystem and buffer spaces for processing the packets arriving along the ingress interfaces and awaiting transmission at the egress interfaces. The switch fabric provides the sufficient bandwidth for transferring packets among different line cards. It is used to receive data from the ingress line-card interfaces and switch it to appropriate egress one(s).

- The control plan is responsible for routing related control functions, such as generating the network map, the way to treat packets according to the different service classifications and discard certain packets. The control plan manages the routing functions, which involve communicating with other network devices, via routing protocols such as Open Shortest Path First (OSPF), to establishing the routing tables. Routing engine cards represent the control plane elements, which run control plane protocols to populate and update the forwarding (IP and MAC address) tables.
- The environmental units are constituted of the elements that do not play a role in handling data traffic, such as the chassis power supply, fans (or air cooling), etc.

As pointed out by Tucker et al. in [10], network devices networking in the different network portions play a central role, since they are major contributors to the energy consumption of modern networks, and the overall energy consumption in networks arises from their operational power requirements and their density. In more detail, operational power requirements arise from all the hardware (HW) elements realizing network-specific functionalities, like the ones related to data and control planes, as well as from HW elements devoted to auxiliary functionalities, such as power supply, air cooling, etc.. In this respect, the data plane certainly handles the most energy-starving and critical component in the largest part of network device architectures, since it is generally composed of special-purpose HW elements (packet processing engines, network interfaces, etc.) that have to perform per-packet forwarding operations at very high speeds. It has been reported in [43; 44] that LCs in the data plane consume about 70% of the total router power, and the Network Processor Units (NPUs), where packet processing engines are used, consume more than 50% of the power consumed by one line card (LC). Focusing on high-end IP routers, Tucker et al. [10] estimated that the power consumed by the data plane weighs for 54% of the total, vs. 11% for the control plane and 35% for power and heat management, as shown in Figure. 2.1. The same authors further broke out energy consumption sources at the data-plane on a per-functionality basis. Internal packet processing engines require about 60% of the power at the data plane of a high-end router, network interfaces weigh for 13%, switching fabric for 18.5% and buffer management for 8.5%. These valuable resulting estimations provide a relevant and clear indication on how and where future research efforts need to be focused in order to build next-generation green devices [14].

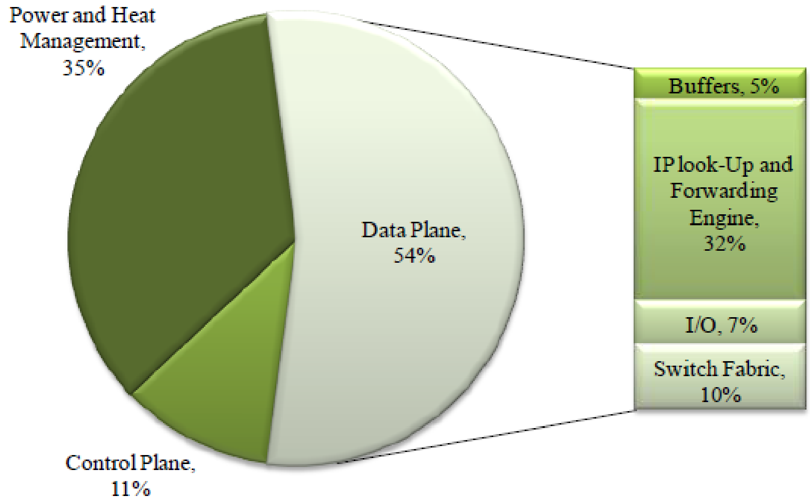

Figure 2.1: Estimation of power consumption sources in a generic platform of high-end IP router [10].

2.2 TOWARD ENERGY- AND QOS-AWARE NETWORK DEVICES

With the rapid growth in the bandwidth of communication links for wired networks, new powerful packet switches and routers are being designed with increasing capacities and performance by exploiting recent improvements in semiconductor technologies. However, the power efficiency of the underlying technology is starting to plateau [3]. The slowing-down of power savings due to technology improvements will lead to the increase in power density. At the same time, the heat dissipation demands of routers are reaching the limits of traditional solutions based on air cooling. Furthermore, current router architectures are not energy aware, in the sense that their energy consumption does not scale sensibly with the traffic load. Therefore, effective and efficient power management in networking equipment is presenting a fundamental challenge to continued bandwidth scaling on the Internet. Chabarek et al. in [3] analyzed two router architectures and evaluated their energy consumption under different traffic loads. The results show that the energy consumption between an idle and a heavily loaded router (with 75% of offered traffic load) vary only of 3% (about 25 W on 750 W). This happens because the router line cards, which are the most power-consuming elements in a router, are always powered on even if they are totally idle. On the contrary, the energy consumption decreases to just 50% if the idle line cards are physically disconnected according to [3]. Such a scenario suggests that future router architectures will be energy aware, which means that they will be able to automatically switch off or dynamically slow down subsystems (e.g. line cards, input/output ports, switching fabrics, and buffers) according to the traffic loads in order to save energy whenever possible. Therefore, energy-efficiency is the first improvement that leads to energy saving through technological innovations without affecting the performance. Such solutions are usually referred as eco-friendly solutions. While energy-awareness is the next improvement toward eco-sustainability, it refers to an intelligent technique that adapts the behavior or performance of the system to minimize its energy consumption [1]. Furthermore, the fundamental problem of greening the Internet is to strike a fine balance between the demands of performance and the limitations of energy usage. Consequently, it has become a trend that the new smarter and more effective strategies enable energy awareness in the Internet architecture, taking into account the tradeoff between energy saving and network performance. Therefore, in order to realize the green Internet, an energy-oriented approach needs to define a comprehensive solution encompassing energy-efficient, energy-aware and QoS-aware aspects.

2.3 DYNAMIC POWER MANAGEMENT TECHNIQUES FOR WIRED NETWORK RESOURCES

In the following, the main dynamic power management techniques are detailed. Besides, the exiting power/energy modeling and measuring techniques also are introduced. Using a generic power/energy model along with these power management techniques, researchers can further explore the potential impact of energy-awareness in wired communication networks.

2.3.1 Power Scaling Techniques

Power scaling techniques are aimed at achieving dynamic power management through modulating capacities of network devices resources (e.g. links bandwidths, computational capacities of packet processing engines, etc.) or turning off unneeded devices (or their subsystems) according to current traffic loads and service requirements.

2.3.1.1 Current Approaches and Concepts In general, the largest part of undertaken approaches is founded on few base concepts, which have been generally inspired by energy-saving mechanisms and dynamic power management criteria that are already partially available in computing systems. These base concepts can be categorized as Dynamic Adaptation and Smart Standby.

- **Dynamic Adaptation (or Speed Scaling)** approaches allow to modulate capacities of packet processing engines and of network interfaces according to the current traffic load and service requirements. This can be performed by using two power-aware techniques, namely, Adaptive Rate (AR) and Low Power Idle (LPI). Adaptive Rate allows a dynamic reduction of the device working rate by tuning the packet processing engine frequency or voltage. The result is a reduction of the power consumption, at the price of lower performance. Low Power Idle, instead, allows reducing power consumption by putting sub-components into low power states when not sending/processing packets, and waking them up as rapidly as possible when the system needs their activity. In detail, the highest rate provides the most energy-efficient transmission while low power idle consumes the minimal power. Both AR and LPI are implemented by pre-selecting a set of HW configuration that can provide different trad-offs between between packet service performance and power consumption. In a sense, AR and LPI might be jointly exploited to better fit system requirements. It is worth noting that the effectiveness of these methods strictly depends on the traffic and network characteristics. For example, the application of LPI capabilities show better results when incoming traffic presents a high burstiness, so that the system has enough time to spend in an idle state before a new burst is received.

- **Smart Standby (or Sleep Mode)** approaches can be considered as deeper idle state: using power management primitives, devices can be turned off smartly and selectively, providing higher power saving than idle states at the price of longer wake up times [45]. The main issues with this approach is represented by the loss of network connectivity. In fact, when a device is sleeping, it cannot be seen on the network, thus a wake up time includes a re-connection phase, in which the device has to send signaling traffic to communicate its presence on the network and allow updating the forwarding tables. This is probably the predominant reason why the networking devices are left fully powered even when not employed. Recent solutions propose the introduction of a proxy to take charge of the host network presence during sleeping times, standby modes have to be explicitly supported with special proxying techniques able to maintain the "network presence" of sleeping nodes or components [46].

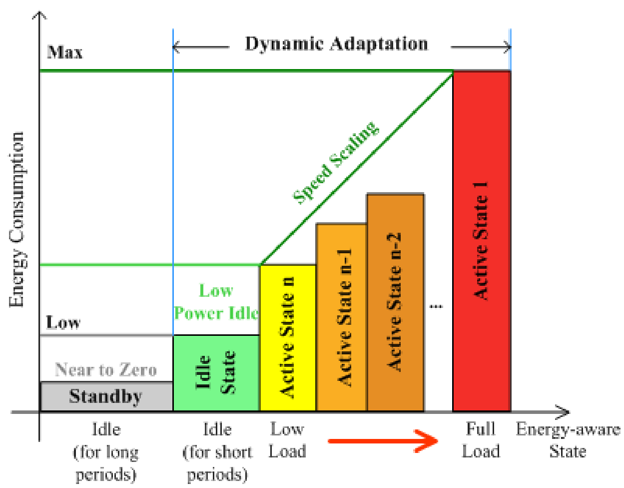

Figure 2.2: Energy-aware Profiles [47].

Dynamic adaptation approaches will enable to modulate energy absorption according to the actual workload through slowing down hardware (HW) components. While approaches based on sleep mode will help to further cut power consumption of unused devices (or parts of them) by shutting down them. All these approaches are not mutually exclusive, and their joint adoption may eventually impact on next-generation network devices by providing "energy-aware" profiles, as depicted in Fig. 2.2. Since these approaches are founded on the idea of either tuning device processing/transmission capacities, or of waking up the hardware upon "active" request or their combinations. The adoption of such green optimizations or their combinations obviously affect network performance, the trading energy consumption for network performance is paid more and more attentions by network researchers.

2.3.1.2 Dynamic Voltage/Frequency Scaling Nowadays, although the largest part of today's network equipment does not include such HW power saving capabilities, power management is a key feature in today's processors across all market segments. This is usually accomplished by scaling the clock frequency or by throttling the CPU clock, we call this technology as dynamic voltage/frequency scaling (DVFS). As one of the most promising energy-efficient technologies, DVFS is becoming an integral part of networks for saving power. In detail, power scaling capabilities allow dynamically reducing the working rate of processing engines or of link interfaces, thereby achieving the purpose of energy saving. With DVFS technology, a CMOS-based processor can operate at different voltages/frequencies to reduce the dynamic power consumption, defined by φ^D, which can be roughly characterized as follows [18; 19]:

$$\varphi^D = a \cdot V_{DD}^2 \cdot f \cdot C \tag{2.1}$$

where a $(0 \leq a \leq 1)$ is the switching activity factor, i.e. the switching activity for each clock tick, and can be considered to be the utilization of the component, V_{DD} is the supply voltage of the processor, f is the clock frequency of the processor, and C is the effective switched capacitance constant. For an efficient control and smooth application of DVFS, a proportionately linear relationship is expected between the frequency and applied voltage [20; 48], thus, the dynamic power consumption can be modeled in terms of frequency like:

$$\varphi^D = \gamma \cdot f^3 \tag{2.2}$$

where γ is a constant parameter.

2.3.2 Power/Energy Measuring Techniques

How to measure and model the power/energy consumption is another big issue for power management of wired networks, various solutions have been proposed in the literature to evaluate at different levels the energy processors consume. Considering a set of power scalable network components, this section introduces several basic techniques used to model/measure power/energy consumption.

2.3.2.1 Power measurement When discussing power issues, two main aspects impacting power consumption need to be considered. The first, referred to as static power, arises from the bias and leakage current to support control plane, environment units, and load-independent data plane [10; 42]. The second, referred to as dynamic power, results from the charging and discharging of the voltage saved in node capacitance of the circuit. Using Φ^S and Φ^D to denote static and dynamic power, respectively, the power Φ consumed by a router can be expressed as follows:

$$\Phi = \Phi^S + \Phi^D \tag{2.3}$$

According to [42], the power consumption of an IP router is the sum of the power consumed by its three major subsystems: namely control plane, environmental units and data plane. Assume that $\Phi_{control}$ denotes the static power consumed by control plane, $\Phi_{environment}$ denotes the static power consumed by environment units, Φ^S_{data} denotes the static power consumed by the constant baseline components in data plane, and Φ^D_{data} denotes the dynamic power consumed by the traffic load dependent components in data plane. Accordingly, the above power components can be further expressed as:

$$\begin{aligned} \Phi^S &= \Phi_{control} + \Phi_{environment} + \Phi^S_{data} \\ \Phi^D &= \Phi^D_{data} \end{aligned} \tag{2.4}$$

2.3.2.2 A general power-aware model for router power consumption Joseph Chabarek et al. in [3] performed several experiments to measure energy consumption of two different Cisco router. Both of them include their base systems (Chassis plus router processor) and line cards, based on which it provides a generic model for router power consumption, as described in Eq. 2.5. In this model, the power consumption Φ of a router is determined by its configuration and current use. The vector X defines the chassis type of the device, the installed line cards and the configuration and traffic profile of the device. The function $\Phi^S(x_0)$ returns the power consumption of a particular chassis type, which is from control plan and environment unit, N is the number of line cards that are active, $\varphi^D_{data}(x_{i0})$ is the dynamic cost with a scaling factor corresponding to the traffic utilization on the router, and $\varphi^S_{data}(x_{i1})$ gives the cost of the line card in a base configuration. The cost of traffic is dependent on the configuration of the router and the amount of traffic. This model is used to formulate the optimization problem for power-aware network design.

$$\begin{aligned}\Phi(X) =& \Phi^S(x_0) + \sum_{i=0}^{N}(\varphi^D_{data}(x_{i0}, x_{i1}) + \varphi^S_{data}(x_{i1})) \\ =& \underbrace{\Phi^S(x_0) + \sum_{i=0}^{N}\varphi^S_{data}(x_{i1})}_{\Phi^S} + \underbrace{\sum_{i=0}^{N}\varphi^D_{data}(x_{i0}, x_{i1})}_{\Phi^D}\end{aligned} \tag{2.5}$$

3.0 DVFS-BASED POWER MANAGEMENT AND QOS-AWARE SCHEDULING STRATEGIES

Excessive reduction in execution speeds to save energy could result in QoS violation of the supported applications. In to address this energy-QoS dichotomy, we, firstly, explore how to design effective DVFS-based, QoS-aware packet scheduling schemes, the objective is to minimize the energy consumption through speed scaling techniques, while achieving a balance between the processor execution rate and the packet delay [40; 41]. The major contributions of this work are: (i) the design of three families of QoS-aware packet schedulers, based on queue length, link utilization and packet delay, respectively. Variants in each family, which differ in when and how decisions are made to adjust the execution rates, are derived; (ii) a holistic simulation framework, including an energy model, is proposed to investigate and compare the performance of each scheme, in different networking environments and traffic models; and (iii) a thorough performance study focusing on the energy consumption and network delay, for each scheduling scheme in each family, is carried out.

3.1 DVFS-SCHEDULER DESIGN AND ARCHITECTURE

The DVFS-Scheduler dynamically adjusts processor frequency, based on the current state of the network, to reduce energy while meeting QoS performance. To design a QoS-aware, energy-efficient strategy for speed-scaling, several issues must be addressed. The first issue is related to monitoring network traffic to determine current network congestion. This information is used to adjust processor frequency, accordingly. When the congestion is high, the frequency must be scaled up, in order to meet the QoS requirements of the application. When the network congestion is low, however, the frequency is scaled down to reduce energy consumption, without violating QoS performance. The second issue deals with accurately determining the congestion granularity and time scale needed to effectively manage frequency scaling. A finer congestion granularity measured over a short time scale leads to higher accuracy, but at the expense of additional overhead. A tradeoff between granularity, time scale and overhead must, therefore, be worked out to achieve accuracy while maintaining low overhead. The third issue deals with the scheduler aggressivity, when scaling the processor's frequency up or down. An aggressive strategy to lower processor speed to save energy, when the network congestion is low, may lead to violation of QoS performance. Similarly, an aggressive strategy to increase processor speed in response to a high burst of traffic, may lead to energy waste. The strategy must, therefore, achieve the right balance between saving energy and adhering to QoS performance.

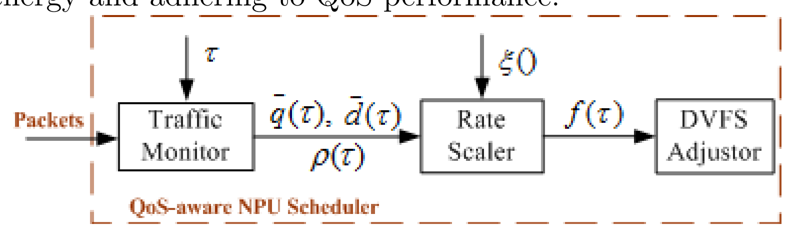

Figure 3.1: DVFS-Scheduler basic architecture.

To address the above issues, a DVFS-based scheduling architecture, depicted in Fig. 3.1, is proposed. The architecture has three main components: Traffic Monitor (TM), Rate Scaler (RS) and DVFS Adjustor (DA). The TM component monitors the packets, over an interval τ, and compute the statics related to the state of the network. Depending on the scheduling strategy, the queue length, $q(\tau)$, or the link utilization, $\rho(\tau)$, are used to scale up or down the Network Processor Unit (NPU) execution rates. The RS component computes a network state-dependent scaling function, $\xi()$, which takes into consideration the aggressivity factor of the scheduling strategy, η, and the current level of network congestion. The scaling function is used by the DA component to adjust the NPU frequency, $f(\tau)$.

Motivated by our research work on DVFS-based dynamic power management, we developed three families of DVFS-based packet scheduling schemes to reduce energy consumption of routers based on different strategies, operating under different traffic loads and network

Table 3.1: Packet Scheduling Schemes.

Family	Scheme	Metric	Scaling Factor	Scaling Strategy
Load-aware [40]	LA	Average traffic Load	ρ	$f(\tau_k) = max\,(f_{min}, min(f_{max} \cdot \rho(\tau_k), f_{max}))$
	$\bar{\text{L}}$A	Predicted traffic Load	$\overline{\rho}$	$f(\tau_k) = max\,(f_{min}, min(f_{max} \cdot \overline{\rho}(\tau_k), f_{max}))$
QL-aware [40]	sQLA	Current Queue Length	$(\frac{q+1}{Q+1})^{\eta}$	$f(\tau_k) = max\left(f_{min}, f_{max} \cdot (\frac{q(t_k)+1}{Q+1})^{\eta}\right)$
	s$\bar{\text{Q}}$LA	Predicted Queue Length (EWMA[1])	$(\frac{\overline{q}+1}{Q+1})^{\eta}$	$f(\tau_k) = max\left(f_{min}, f_{max} \cdot (\frac{\overline{q}(\tau_k)+1}{Q+1})^{\eta}\right)$
	mQLA	Current Queue Length	$(\frac{(q-ql)+1}{(qh-ql)+1})^{\eta}$	$f(\tau_k) = \begin{cases} f_{min}, & \text{if } q(t_k) \leq ql \\ f_{max}, & \text{if } q(t_k) > qh \\ f_{min} + (f_{max} - f_{min}) \cdot (\frac{(q(t_k) - ql) + 1}{(qh - ql) + 1})^{\eta}, \\ \text{if } ql < q(t_k) \leq qh \end{cases}$
	m$\bar{\text{Q}}$LA	Predicted Queue Length (EWMA)	$(\frac{(\overline{q}-ql)+1}{(qh-ql)+1})^{\eta}$	$f(\tau_k) = \begin{cases} f_{min}, & \text{if } \overline{q}(\tau_k) \leq ql \\ f_{max}, & \text{if } \overline{q}(\tau_k) > qh \\ f_{min} + (f_{max} - f_{min}) \cdot (\frac{(\overline{q}(\tau_k) - ql) + 1}{(qh - ql) + 1})^{\eta}, \\ \text{if } ql < \overline{q}(\tau_k) \leq qh \end{cases}$
Delay-aware [41]	QLDA	Predicted Queue Length & Packet Delay (EWMA & GPR[2])	$(\frac{\overline{q}-ql}{qh-ql})^{\eta(\rho)}$	$f(\tau_k) = \begin{cases} f_{min}, & \text{if } \overline{q}(\tau_k) \leq q_l \\ f_{max}, & \text{if } \overline{q}(\tau_k) > q_h \\ f(\tau_{k-1}), \\ \text{if } q_l < \overline{q}(\tau_k) \leq q_h \text{ and } \left\lvert \overline{d}(\tau_k) - d^T \right\rvert \leq \tilde{d}v(\tau_k) \\ f_{min} + (f_{max} - f_{min}) \cdot (\frac{\overline{q}(\tau_k) - ql}{qh - ql})^{\eta(\rho(\tau_k))}, \\ \text{if } q_l < \overline{q}(\tau_k) \leq q_h \text{ and } \left\lvert \overline{d}(\tau_k) - d^T \right\rvert > \tilde{d}v(\tau_k) \end{cases}$

topologies under the same QoS constraints, as summarized in TABLE 3.1. Using DVFS, routers can adaptively adjust the operational frequency of their processors, based on current conditions of the network. Two metrics are considered, namely current queue length and link utilization, are considered to achieve this goal.

The first family of schemes studied in this research project uses the network traffic load, i.e. link utilization, to dynamically scale the processor's speed [1]. The first Load-based scheme, referred to as Load-aware scheduler (LA), uses the traffic load over packet inter departure interval to adjust the NPU frequency. The second scheme, referred to as predicted Load-aware scheduler ($\bar{\text{L}}$A), uses the predicted average load by exponentially weighted moving average (EWMA) algorithm over a given interval time, to adjust the frequency. In this family, when the load is high, the speed is scaled up, and when the load is low, the speed is scaled down.

The second family of schemes, referred to as Single-threshold, QL-aware scheduler (sQLA), Multi-threshold, QL-aware Scheduler (mQLA), Single-threshold Average QL-aware Scheduler (s$\bar{\text{Q}}$LA) and Multi-threshold Average QL-aware Scheduler (m$\bar{\text{Q}}$LA) [1], uses the queue length, instead of link utinlization, to scale the frequency [40]. When the queue length increases, the scheduler scales the frequency up to meet the QoS delay requirements. When the queue length decreases, however, the scheduler scales the frequency down to save energy, without violating the QoS requirements. sQLA and mQLA use instantaneous queue length when adjusting NPU frequency. As such, they are instantly responsive to traffic load variation. Insights derived from these schemes are valuable in gaining better understanding of the energy saving levels that can be achieved. These schemes, however, are not feasible in real networks, due to the overhead caused by excessive frequency adjustments. A practical implementation of these schemes can be achieved by using the average, as opposed to the instantaneous, queue length. Therefore, the resulting average queue-length based schemes, s$\bar{\text{Q}}$LA and m$\bar{\text{Q}}$LA, both use the EWMA algorithm to estimate the queue length periodically over a given interval to dynamically adjust processor frequencies.

The third family scheme, Queue Length (QL)-based, Delay-aware packet scheduler (QLDA) [41], is an extended scheme of m$\bar{\text{Q}}$LA [40]. It uses multiple queue length thresholds to accurately capture network congestion. In response to different levels of network congestion, different NPU-rate scaling strategies are used to determine when and how NPU execution rates are adjusted based on the predicted queue length and the estimated delay variance, aiming to achieve adequate energy savings under different traffic loads, without degrading delay performance. Besides, using Gaussian regression model to generate the aggressivity factor of the scheduling strategy based on the traffic load is another improvement of m$\bar{\text{Q}}$LA. Therefore, QLDA displays more efficient and sufficient on balancing high energy saving and QoS requirements compared with m$\bar{\text{Q}}$LA.

3.2 EVALUATION

A simulation framework to assess the performance of the energy- and QoS-aware scheduling schemes discussed above is proposed in [40; 41]. We consider a set of DVFS-enabled routers and present a detailed model to determine the *packet-based* and *router-based* energy consumption, taking into consideration the frequency adjustment strategy used by the underlying scheduler. A NS2-based simulation framework is used to assess the performance of the proposed strategies in terms of energy gain.

3.2.1 Packet- and Router-based Energy Consumption Models

Two main components impact power consumption in network routers [42; 19]. The first, referred to as static power, arises from the bias and leakage current to support control plan, environment units, and load-independent data plan [42]. The second, referred to as dynamic power, results from the charging and discharging of the voltage saved in node capacitance of the circuit. We use Φ^S and Φ^D to denote static and dynamic power, respectively. In a router, NPUs operate in two possible states, namely "idle" and "busy". In the "idle" state, the power consumption is load-independent and equals to the static power, Φ^S. In the "busy" state, the power consumption is load-dependent and is composed of the static power Φ^S and dynamic power Φ^D. Consequently, the power consumed by a router can be expressed as follows:

$$\Phi = \begin{cases} \Phi^S, & \text{"idle" state} \\ \Phi^S + \Phi^D, & \text{"busy" state} \end{cases} \tag{3.1}$$

The dynamic power, Φ^D, can be further expressed as $\Phi^D = \gamma \cdot f^3$ [20; 48]. The parameter f denotes the clock frequency of the NPU processor and γ is a constant parameter, expressed in units of $Watts/GHz^3$.

3.2.1.1 Packet-based Energy Model

For a given router, the dynamic power consumed by the data plane, Φ^D, is composed of two components, namely the *per-packet processing power* component, Φ_P, and the *per-byte store and forward power* component, $\Phi_{S\&F}$ [42]. Both components are affected by the operational processor frequency, f. Φ_P represents the power consumed to process a given packet, regardless of the packet payload size. $\Phi_{S\&F}$, on the other hand, represents the power needed to receive, store, switch and transmit a packet. Contrary to Φ_P, which only depends on the number of instructions needed to process a packet (IPP_P), $\Phi_{S\&F}$ depends on the packet length, as packets with different lengths require different storage, switching time and transmission time, thereby consuming different amounts of power.

Let $IPB_{S\&F}$ denote the number of instructions required to process, store and forward a byte worth of data. Assuming a packet length of L *bytes*, the number of instructions required to process the packet is $IPP_{S\&F} = L \cdot IPB_{S\&F}$. Note that $IPB_{S\&F}$ is constant, as it only depends on the number of instructions to process a byte. Therefore, IPP_P can be expressed as a linear function of $IPB_{S\&F}$, namely $IPP_P = h \cdot IPB_{S\&F}$, where $h > 0$.

Let IPP represent the number of instructions to complete the processing, store, switch and transmission an entire packet with length L by a NPU at a given LC. We have $IPP = IPP_P + IPP_{S\&F} = (h+L) \cdot IPB_{S\&F}$. The NPU's processing, storage, switching and transmission time of a packet, $T_p = \frac{IPP}{IPS}$, where IPS represents the number of instructions executed by the NPU per second. IPS can be further expressed as $\frac{f}{CPI}$, where f denotes the operational frequency of the NPU and CPI represents the number of cycles per instruction. Therefore, $T_p = \frac{IPP \cdot CPI}{f} = \frac{\Theta \cdot (h+L)}{f}$, where $\Theta = CPI \cdot IPB_{S\&F}$.

Let $f_{j,i}$ denote the operational frequency of the active NPU j in LC i. In practice, the NPU only allows a number of manufacturer-specified discrete operational voltage levels, $V = \{V_1, ..., V_l, ..., V_M\}$. These discrete levels result in a corresponding set of discrete frequencies, $F = \{f_1, ..., f_l, ..., f_M\}$. Consequently, $f_{j,i}$ must be set to the smallest discrete frequency, $f_l (1 \leq l \leq M) | f_l \geq f_{j,i}$. The dynamic energy consumed by a successful packet transmission with length L at NPU j in LC i is given by:

$$E^D_{j,i}(T_p) = \underbrace{\gamma_{j,i} \cdot f^3_{j,i}}_{\varphi^D_{j,i}} \cdot T_p = \gamma_{j,i} \cdot \Theta_{j,i} \cdot f^2_{j,i} \cdot (h_{j,i} + L) \tag{3.2}$$

3.2.1.2 Router-based Energy Model Assume that a router is equipped with Ψ LCs, each LC_i $(1 \leq i \leq \Psi)$ is equipped with n_i active NPUs. Let $T^B_{j,i} = \sum_{\forall} p T_p$ $(1 \leq j \leq n_i$ and $1 \leq i \leq \Psi)$ denote the busy time interval during which NPU j in LC i processes, stores, switches and transmits packets over the entire router's operation time, T, which includes idle and busy periods. The energy consumption of the router, over T, can be expressed as $E(T) = E^S(T) + E^D(T^B)$, where $E^S(T)$ represents the energy consumed due to static power during T and $E^D(T^B)$ represents the energy consumed due to dynamic power over the busy period, T^B. These energy components can be expressed as:

$$\begin{aligned} E^S(T) &= \Phi^S \cdot T \\ E^D(T^B) &= \sum_{i=1}^{\Psi} \sum_{j=1}^{n_i} E^D_{j,i}(T^B_{j,i}) \end{aligned} \tag{3.3}$$

$E^D_{j,i}$ represents the energy consumption by NPU j in LC i due to dynamic power, over the busy period, $T^B_{j,i}$. Note that $E^D_{j,i}$ depends on the dynamically changing frequencies used to process, store, switch and transmit a given packet, based on the scheduler's scaling decision.

Let $Z_{j,i}$ be the amount of time intervals at NPU j in LC i over time T, and $\tau_1, \cdots, \tau_k, \cdots, \tau_{Z_{j,i}}$, $1 \leq k \leq Z_{j,i}$, represent the frequency time slots at NPU j in LC i. Assuming $f_{j,i}(\tau_0)$ is the initial frequency. The frequency of NPU j at LC i, over the time interval τ_k, is $f_{j,i}(\tau_{k-1})$, where $1 \leq i \leq \Psi$, $1 \leq j \leq n_i$ and $1 \leq k \leq Z_{j,i}$. Let $D_{j,i}(\tau_k)$ denote the number of packets serviced by NPU j in LC i over the time interval τ_k. According to Eq. 3.2, the total dynamic energy consumed by $D_{j,i}(\tau_k)$ packets over the busy period $T^B_{j,i}(\tau_k) = \sum_{p \in D_{j,i}(\tau_k)} T_p$ during the time interval τ_k can be expressed as:

$$E^D_{j,i}(T^B_{j,i}(\tau_k)) \;=\; \gamma_{j,i} \cdot \Theta_{j,i} \cdot f^2_{j,i}(\tau_{k-1}) \cdot D_{j,i}(\tau_k) \cdot (h_{j,i} + \overline{L}_{j,i}(\tau_k)) \tag{3.4}$$

The parameter $\overline{L}_{j,i}(\tau_k)$ represents the average length of the packets serviced at NPU j in LC i over the interval τ_k. The energy consumed by the router over the total operational period, $T = \sum_{k=1}^{Z_{j,i}} \tau_k$, is derived in Eq. 3.5.

$$E(T) = P^S \cdot T + \sum_{i=1}^{\Psi} \sum_{j=1}^{n_i} \sum_{k=1}^{Z_{j,i}} \gamma_{j,i} \cdot \Theta_{j,i} \cdot f^2_{j,i}(\tau_{k-1}) \cdot D_{j,i}(\tau_k) \cdot (h_{j,i} + \overline{L}_{j,i}(\tau_k)) \tag{3.5}$$

To validate the above router energy model, without loss of generality, we derive the total energy consumed by a router for two special cases: the first case assumes a set of Ψ homogeneous LCs, while the second assumes all LCs have the same number of active NPUs. Note that, in both cases, the packet energy consumption can be expressed as $E_p = EP_P + EB_{S\&F} \cdot \overline{L}$, where EP_P, expressed in $nJ/packet$, denotes the per-packet processing energy, and $EB_{S\&F}$, expressed in $nJ/byte$, denotes the per-byte store and forward energy, and $\overline{L}$ is the average packet length [42].

Using the above model, we can derive an expression for h and γ, for a homogeneous network. Let $EB_{P_{max_{j,i}}} = EP_{P_{max}}$, $EB_{S\&F_{max_{j,i}}} = EB_{S\&F_{max}}$, $f_{max_{j,i}} = f_{max}$. Consequently, $h_{j,i} = h$, $\gamma_{j,i} = \gamma$, $\Theta_{j,i} = \Theta$, where $1 \leq j \leq n_i$, $1 \leq i \leq \Psi$. According to Eq. 3.2, we can compute $h = \frac{EP_{P_{max}}}{EB_{S\&F_{max}}}$ and $\gamma = \frac{EB_{S\&F_{max}}}{\Theta \cdot f_{max}^2}$. The router total energy for the simple homogeneous case is expressed in Eq. 3.6. The same method can be used to compute $\gamma_{j,i}$ and $h_{j,i}$, for a network of heterogeneous LCs.

$$E(T) = P^S \cdot T + \sum_{i=1}^{\Psi} \sum_{j=1}^{n_i} \sum_{k=1}^{Z_{j,i}} \frac{f_{j,i}^2(\tau_{k-1})}{f_{max}^2} \cdot D_{j,i}(\tau_k) \cdot (EP_{P_{max}} + EB_{S\&F_{max}} \cdot \overline{L}_{j,i}(\tau_k)) \tag{3.6}$$

Suppose that each LC has the same number of active NPUs. Furthermore, assume that all NPUs in LCs synchronously process their incoming traffic with average packet length $\overline{L}$, use the same speed-scaling strategy over the operational time interval, T. We set $Z_{j,i} = Z$, $n_i = n$, $\overline{L}_{j,i} = \overline{L}$ and $D_{j,i}(\tau_k) = D(\tau_k)$, where $1 \leq j \leq n$, $1 \leq i \leq \Psi$, $1 \leq k \leq Z$. The above energy model in Eq. 3.6 can be further simplified to:

$$E(T) = P^S \cdot T + \Psi \cdot n \cdot \frac{(EP_{P_{max}} + EB_{S\&F_{max}} \cdot \overline{L})}{f_{max}^2} \cdot \sum_{k=1}^{Z} f^2(\tau_{k-1}) \cdot D(\tau_k) \tag{3.7}$$

Eq. 3.6 and Eq. 3.7 demonstrate that adjusting the frequency, as opposed to using the maximum frequency, further reduces energy consumption. The following simulation study will be used to further determine the impact of dynamically adjusting frequencies on energy consumption.

3.2.2 Simulation Setup

In our simulation framework, we consider two network topology models: i.e. *dumbbell* and *parking lot*, which are two promising models to capture the behavior and performance of a large variety of Internet applications [49; 50; 51; 52]. In the topology models, the capacities of links between all the routers are 10 *Gbps*. The routers implement FIFO scheduling and DropTail queuing. The propagation delays between the sources and the destinations are 40 *ms*, which is equivalent to the time the light travels from the east coast to west coast. In each router, all LCs are configured with multiple NPUs, each using a specific QoS-aware DVFS scheduler. In order to simulate real scenarios, Huawei CX600-X3 Metro

Router model [42], supporting $10GE$ LCs, is used. We further assume that each $10GE$ port provides 250 ms worth of traffic buffering. This results in processor buffers of approximately $250ms \times 10Gbps$, which is roughly 250000 packets, assuming the average packet size of 1250 bytes. The range of operating frequencies, $[1.6GHz,\ 2.4GHz]$, for a given NPU, is based on Intel XEON DPDK specification [53]. TABLE 3.2 describes the main simulation parameters used in this simulation study. According to [54; 55], TABLE 3.3 specifies three traffic source models, namely one constant bit rate (CBR) model: CBR Video, and two variable bit rate (VBR) models: VBR VoIP and VBR Data, which satisfy Pareto and Exponential On/Off distribution, respectively.

Table 3.2: Main simulation parameters and conditions.

Items	Simulation Parameters	Simulation Conditions
Router	Router Node	Metro Router [42]
	NIC port	$10GE$
	Operating Frequency (GHz)	$1.6 \sim 2.4$
	$CPI(cycles/instruction)$	1.2
	$EP_{P_{max}}(nJ/pkt)$	1375 [42]
	$EB_{S\&F_{max}}(nJ/byte)$	14.4 [42]
	$P^S(Watts)$	352 [42]
Packet	Packet Max size (bytes)	1500
	$IPB(instructions/byte)$	1.5
Queue	Service Discipline	FIFO
	Queuing Management Discipline	DropTail
Network	Topology Model	3-hop dumbbell
		4-hop parking lot
	Network Traffic *Load*	$0.5, \cdots, 0.9$
	Propagation Delay (ms)	dumbbell: 40; parking lot: 40
	Traffic Model	Video:VoIP:Data

Table 3.3: Traffic source models and specifications.

Flow Type	Load Percentage	T_{On} (ms)	T_{Off} (ms)	Peak Rate	β
Video	50%	NA	NA	$10Mbps$	NA
VoIP	20%	400	400	$64Kbps$	1.1
Data	30%	40	360	$256Kbps$	NA

The ITU G.114 specification recommends less than 150 ms one-way end-to-end delay for high-quality real-time traffic such as voice and video. In order to assure a good quality of the above traffic models, measures of the QoS parameters must respect the following values [56; 57; 58]. In our simulation, we consider the following QoS requirements to evaluate energy saving percentage (ESP), average end-to-end delay (AED) for all discussed QoS-aware schemes.

- 150 ms as the average end-to-end delay threshold (AEDT) [57],
- 30 ms as the delay jitter bound (DJB),
- 1% as the packet loss rate (PLR) threshold.

3.2.3 Result Summaries

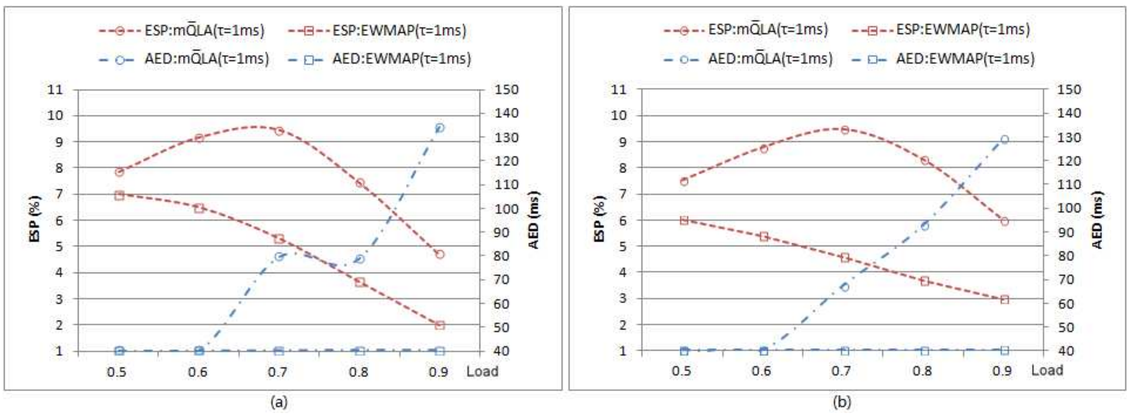

Figure 3.2: ESP and AED comparisons between m$\bar{\text{Q}}$LA [40] ($\eta = 0.15$, $q_l : q_h = 4\% : 80\%$) and EWMAP [18] ($w_a = 0.2$) for (a) dumbbell model, (b) parking lot model.

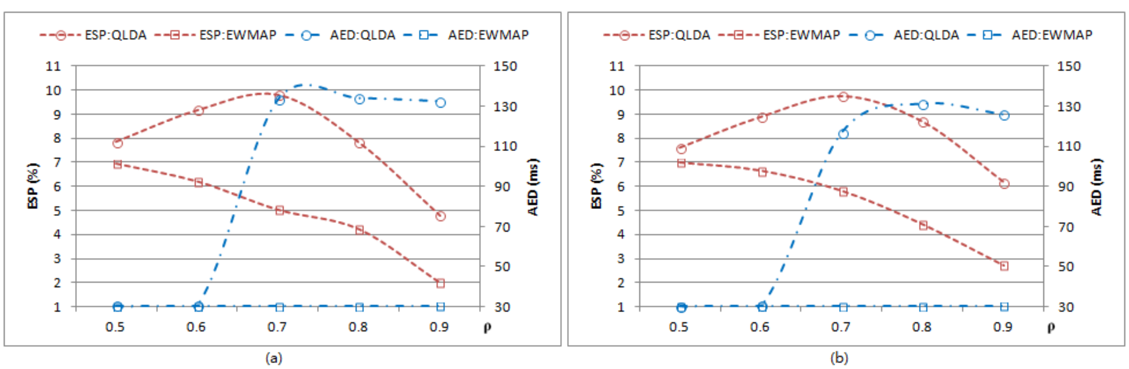

Figure 3.3: ESP and AED comparisons between QLDA [41] ($q_l : q_h = 4\% : 80\%$) and EWMAP [18]($w_a = 0.2$) for (a) dumbbell model, (b) parking lot model.

A thorough analysis of the proposed schemes, using NS2, has been carried out, for different network environments and traffic loads. The objective is to fine tune the main parameters of these schemes to achieve the balance between the energy minimization and the QoS requirements [40; 41]. The simulation results show that all QoS-aware DVFS-based schemes have potential for significant energy saving in high-speed networks, with acceptable delay performance, and that QL-aware family schemes achieve, on average, higher energy savings than Load-aware family schemes, whereby the m$\bar{Q}$LA scheme achieves the best results among these two basic families, with performance gains of up to 9.5% energy saving, while meeting the QoS performance of the supported applications, as shown in Fig.3.2 [40]. Furthermore, as the extension of m$\bar{Q}$LA, QLDA has advantage over m$\bar{Q}$LA, which can achieve up to 10% energy saving while keeping the desired QoS performance, as depicted in Fig.3.3 [41]. In general, it is hard for Load-ware schemes to control the QoS performance accurately, especially in the high traffic load. On the contrary, the QL-aware schedulers and the QL-based, delay-aware scheduler, QLDA, can more accurately control the QoS performance through adjusting queue length thresholds.

3.2.4 Limitations and Further Studies

Compared to the exiting speed scaling solutions, our proposed QoS-aware packet scheduler addresses energy-performance challenge. It not only saves significant energy, but seeks a balanced tradeoff between high network energy savings and acceptable levels of network QoS performance under different traffic loads, based on a comprehensive router-based energy model. This is achieved by controlling the NPU execution rates based on dynamic queue length. In [40; 41], we mainly analysis two simple dumbbell and parking lot network topology models. In the real world, however, there are more realistic and complex topologies. Therefore, given the QoS requirements, the network model, the routing path and the character of traffic load could be important impact factors to the important factors of schedulers. Our future work will further explore these issues. Besides, the energy saving through scaling speed is limited due to the load-dependent power source percentage occupancy among the whole power consumption, creating a intelligent energy-aware strategy by sleep mode to save more energy without QoS violation would be our future goal.

4.0 DVFS-BASED POWER MANAGEMENT AND A LOAD-AWARE, OPTIMAL ENERGY STRATEGY

Among a large number of dynamic power management solutions, a less expensive one is to use mathematical models to formulate the energy saving problem [59]. For DVFS-enabled network components, the energy optimization problem, related to speed scaling, subjects to the conflicting dual objectives of speed scaling and QoS requirements. Therefore, the ability to efficiently manage network resources to minimize the energy consumption is critical to effectively addressing network congestion and end-to-end QoS guarantees. For a given traffic flow, each router along the path must determine the node execution speed at which it must process traffic to minimize energy and meet QoS requirements. To address this issue, we propose a DVFS-based energy optimization framework, and further explore the design and performance assessment of an energy- and QoS-aware strategy to support delay-sensitive applications. More specifically, given a flow specification and a scheduling policy, a per-node *feasible* minimum and maximum delay values are computed. Using these values, the energy- and QoS-aware problem is modeled as a *routing path energy-minimization problem* to determine, for each router along the path, the processing node execution speed and the flow delay that minimize energy without violating the flow's *end-to-end* delay requirement. The main work involves three aspects: (i) the development of a model to compute a node-based energy consumption, taking into consideration both the static and dynamic energy components; (ii) a methodology to compute feasible lower and upper bound delays of a flow, based on the router's current traffic load; (iii) heuristic methods to compute feasible per-node delays that meet the end-to-end delay requirements and minimize energy across the path.

4.1 OPTIMIZATION FRAMEWORK

To minimize the energy consumption of the network components for a given routing path, we build a DVFS-based optimization framework:

$$\begin{aligned}
\min \quad & E(\vec{\delta}, \vec{\sigma}) \\
\text{s.t.} \quad & l_i - \delta_i \leq 0, \quad i = 1, \cdots, K \\
& \delta_i - h_i \leq 0, \;\; i = 1, \cdots, K \\
& \sum_{i=1}^{K} \delta_i - \Delta \leq 0, \\
& \sigma_i \in [\sigma_{i_{min}}, \sigma_{i_{max}}], \;\; i = 1, \cdots, K
\end{aligned}$$

The objective is to address the question of how to efficiently assign per-node delays, $\vec{\delta} = (\delta_1, \cdots, \delta_i, \cdots, \delta_K)$, and per-node execution speeds, $\vec{\sigma} = (\sigma_1, \cdots, \sigma_i, \cdots, \sigma_K)$, to the new flow along a given routing path with nodes, $1, \cdots, K$, to minimize the energy consumption, while adhering to the QoS requirements of the routed applications. l_i specifies a lower bound on the delay values node i can offer to the new flow, based on i's current processing excess capacity and the new flow's requirements. Similarly, h_i denotes the a upper bound on the delay values node i can offer to the new flow. Δ presents the end-to-end delay of the new flow, and $\sigma_{i_{min}}$ and $\sigma_{i_{max}}$ together describe the range of the execution speed, σ_i, at node i.

4.1.1 Node Architecture

In this framework, we present a DVFS-enabled, delay-based scheduling node architecture, which contains a DVFS-based power model, and a node processing capacity service model adopting delay-based scheduling policy, for carrying various multimedia applications. In this architecture, the power model is the basic to further calculate path-based energy consumption, and the node processing capacity model is used to compute the feasible per-node delay bounds for a given new flow.

4.1.1.1 Power Model The dynamic power consumption of a computing node executing at speed, σ, can be roughly characterized as $\varphi^D(\sigma) = \gamma \cdot \sigma^3$. Assume that node processing speed is continuous (restricted to a given interval $[\sigma_{min}, \sigma_{max}]$). In addition to the dynamic power, the bias and leakage current to support control plan, environment units, and load-independent data plane contribute to the static power consumption, which is independent of the processor speed [42; 40]. Define the static power as a fixed fraction of the node power consumed when executing at maximum speed, referred to υ (i.e. static power ratio) [60]. Hence, the power consumption of an active node processor can be expressed as: $\varphi(\sigma) = \upsilon \cdot \sigma_{max}^3 + (1-\upsilon) \cdot \gamma \cdot \sigma^3$.

4.1.1.2 Processing Capacity Service Model In this node architecture, the delay-based scheduling policy is considered, which assigns priorities to flows so that flows with shorter delays have higher priorities than those with longer delays, which is optimal among fixed-priority scheduling algorithms [61]. For a given class of delay-based servers, one can derive a collection of practical and theoretically sound quantitative methods which can be used by the server to assess the feasibility of supporting the requirements of a new flow while continuing to guarantee the requirements of currently supported flows. This can be achieved by computing the utilization of the scheduled activities and comparing it to a schedulable bound which depends on the scheduling policy used by the server [62].

Consider a set of flow, $j = 1, 2, \cdots N_i$, traveling through network node i. Packets from flow j encounters a delay, $\Delta_{j,i}$, at node i. Assume that node i uses a nonpreemptive delay-based scheduling policy to serve packets from different flows with the processor processing rate, σ_i. Then, the support of flows $j = 1, 2, \cdots, N_i$ are feasible at node i if

$$\sum_{j=1}^{N_i} \frac{W_{j,i}}{\Delta_{j,i}} \leq P_{N_i,i} - \frac{\overline{u}}{\underline{\Delta}} \tag{4.1}$$

where $W_{j,i}$ presents the execution time required by flow j over its assigned delay, $\Delta_{j,i}$ at node i. The term $\frac{\overline{u}}{\underline{\Delta}}$, $\overline{u} = max_{1 \leq j \leq N_i} \{u_{j,i}\}$, where $u_{j,i}$ denotes the service time used to process flow j at node i, and $\underline{\Delta} = min_{1 \leq j \leq N_i} \{\Delta_{j,i}\}$ accounts for the nonpreemptive aspect of the packet service at node i. It represents the maximum amount of time a higher priority packet, arriving just at the instant a lower priority packet gained access to the server, may be forced to wait before being serviced [62; 63]. $P_{N_i,i}$ denotes the total percentage of processing capacity which can be allocated to provide guaranteed service to the flow set, $j = 1, 2, \cdots N_i$, at node i. For the delay-based scheduling policy [62], then $P_{N_i,i}{=}N_i \cdot (2^{\frac{1}{N_i}} - 1)$.

The characterization of the above processing service capacity is the basis for the computation of the delay bounds such as l_i and h_i, that can be supported by a node. According to Eq. 4.1 and Eq. 4.5, we can derive the condition of guaranteeing scheduling as Eq. 4.2, based on which we define $l_i = t_i(\sigma_{i_{max}})$ and $h_i = t_i(\sigma_i^{N_i})$ as two bound values of the delay, l_i and h_i, for the new flow, $N_i + 1$, at node i.

$$t_i(\sigma_i^{N_i+1}) = \begin{cases} \dfrac{b_{N_i+1} + 1}{\sigma_i^{N_i+1} \cdot P_{N_i+1,i} - \sum_{j=1}^{N_i} \frac{\Omega_j(\delta_{j,i})}{\delta_{j,i}} - r_{N_i+1}}, & t_i(\sigma_i^{N_i+1}) \leq \underline{\Delta} \\ \dfrac{b_{N_i+1}}{\sigma_i^{N_i+1} \cdot P_{N+1,i} - \sum_{j=1}^{N_i} \frac{\Omega_j(\delta_{j,i})}{\delta_{j,i}} - \frac{1}{\underline{\Delta}} - r_{N_i+1}}, & t_i(\sigma_i^{N_i+1}) > \underline{\Delta} \end{cases} \tag{4.2}$$

A challenge in the above methodology is that the computed value of the upper bound value for the new flow delay, h_i, is hard to guarantee its always positivity. When a new flow connects into the given routing path, the new speed we are trying to find should be greater than and equal to the current speed before the new flow request, if we apply the smaller speed value, i.e. the current speed, into Eq. 4.2, theoretically, we should obtain a larger delay value, and further set it as the new upper bound. But, a potential problem is that with the increasing of the traffic requests, the value of $P_{N+1,i}$ decreases from 1 to 0.667, while the value of $\sum_{j=1}^{N_i} \frac{\Omega_j(\delta_{j,i})}{\delta_{j,i}}$ increases, as a result, the value of delay upper bound, h_i, calculated by using the current speed value could be an infinity or even a negative. Therefore, how to smartly make decision to avoid this satiation becomes critical, that is what we are solving, as shown in Eq. 4.3.

$$h_i = \begin{cases} t_i^{'}(workload), & h_i > t_i^{'}(workload) \text{ } or \text{ } h_i < 0 \\ t_i(\sigma_i^{N_i}), & otherwise \end{cases} \tag{4.3}$$

4.1.2 Energy Computation Model

Considering a set of DVFS-enabled network processors along a given routing path, we explore the *path-based* energy consumption model based on the traffic flow specification.

4.1.2.1 Flow Workload Model Consider a routing node, i, and a flow, j, characterized by a linear bounded arrival processes (LBAP) traffic rate specification vector, (b_j, r_j), where

b_j denotes the maximum packet burst size over any time interval, and r_j presents the long-term average rate of the traffic source. Thus, the maximum number of packets, $\Omega_j(t)$, generated by j, over a time interval of size t, can be expressed as:

$$\Omega_j(t) = b_j + r_j \cdot t, \forall t > 0 \tag{4.4}$$

This load characterization provides an upper bound on the amount of traffic generated by flow j over a time interval δ. Let IPP_i represent the number of instructions to complete the processing, store, switch and transmission of one packet, at node i. Thus, the processor execution rate, μ_i, at node i, can be expressed as: $\mu_i = \frac{\sigma_i}{IPP_i}$. Given the traffic flow specified by j, the maximum amount of service time, $W_{j,i}(t, \sigma_i)$, required by flow j, at node i, over a time interval of size t, can be expressed as:

$$W_{j,i}(t, \sigma_i) = \frac{IPP_i \cdot (b_j + r_j \cdot t)}{\sigma_i} \tag{4.5}$$

4.1.2.2 Path-based Energy Consumption Model For a given node set with size of K along the routing path, we set two vectors for the new flow, $N_i + 1$, at node i ($1 \le i \le K$): namely delay vector $\vec{\delta} = (\delta_{N_i+1,1}, \cdots, \delta_{N_i+1,i}, \cdots, \delta_{N_i+1,K})$ and execution rate vector $\vec{\sigma} = (\sigma_1, \cdots, \sigma_i, \cdots, \sigma_K)$, the path-based energy consumed by all supported flows, over their agreeable delays, can be derived as:

$$\begin{aligned} E^D(\vec{\delta}, \vec{\sigma}) &= \sum_{i=1}^{K} E^D_{j\in[1,N_i]}(\vec{\delta'_i}, \sigma_i) + \sum_{i=1}^{K} E^D_{j=N_i+1}(\delta_{N_i+1,i}, \sigma_i) \\ &= \sum_{i=1}^{K} r_i \cdot \sigma_i^3 \cdot \left(\sum_{j=1}^{N_i} W_j(\delta_{j,i}, \sigma_i) + W_{N_i+1}(\delta_{N_i+1,i}, \sigma_i) \right) \\ &= \sum_{i=1}^{K} (c_i + d_i \cdot \delta_{N_i+1,i}) \cdot \sigma_i^2 \end{aligned} \tag{4.6}$$

where c_i and d_i are two constants.

4.1.3 Load-based, Optimal Energy Strategy

Requests for flow establishment arrive to the network and are processed sequentially. Assume the network receives a request to establish a new flow characterized by its specification vector (b, r) and its end-to-end delay value Δ. Furthermore, assume that the routing path is composed of nodes, $1, \cdots, K$. A load-based, per-node delay and per-node execution speed assignment strategy is said to be optimal if:

- The per-node delay assignments are feasible across the routing path.
- The per-node execution speed assignments are feasible across the routing path.
- The end-to-end delay requirements of the new flow are enforced without violating the delay requirements of the currently supported flows.
- The maximum traffic flow set utilization due to the new flow connection does not affect on the feasibility under the given (i.e. delay-based) scheduling policy.

Based on the DVFS-based energy optimization framework and the load-aware, optimal energy strategy, we can further explore different heuristic methods to seek the feasible schedule to minimize the energy consumption, under QoS constraints.

4.2 EVALUATION

We can evaluate different energy optimization algorithms by simulation in a given network topology, and analyze the their influences on the network energy efficiency through different green metrics.

4.2.1 Simulation Setup

In our simulation framework, we consider an Ethernet network topology G, which contains all router nodes, the connection relationships and network capacity among them. Considering a new request on a given routing path with K nodes in G, based on which a set of simulation experiments were developed and used to compare the energy efficiency of each algorithm.

On the given path, all LCs in each node are configured with multiple NPUs, each using a specific DVFS-enable, delay-based scheduler. We assume the network capacity of all links in the network topology G is 10 $Gbps$. We change the number of flows in the network topology to simulate different traffic load on the given routing path, thus the traffic matrix is randomly generated upon servers. In order to simulate real scenarios, Huawei CX600-X3 Metro Router model [64], supporting 10 GE port, is used. We further assume that each 10 GE port provides 250 ms worth of traffic buffering. We consider a set of flows execute on a processor that is capable of running at continuous speeds in this paper. The range of operating frequencies, $[50, 250]\, MHz$, for a given NPU, is based on CSP SERIES [65]. In all experiments, the profiles of the simulated flows, were generated randomly. Besides, according to ITU G.114 specification, it recommends less than 150 ms one-way end-to-end delay for high-quality real-time traffic such as voice and video [56]. Therefore, we consider the end-to-end delay requirements of the flows were randomly generated from an interval of $[0, 150]$ ms. TABLE 4.1 provides the two green metrics: dynamic energy gain (DEG) over the agreeable delays and power gain (PG), which determine how energy efficiency will be defined. They are analyzed and compared based on the energy or power dissipation of current practice with no DVFS capabilities implemented in any line-card (LC) where all processors operate at maximum frequency.

Table 4.1: Energy-efficient Metrics.

Energy-efficient Metrics	**Definitions**
Dynamic Energy Gain (DEG %) over agreeable delays	$\frac{E^D(\vec{\delta},\vec{\sigma}_{max})-E^D(\vec{\delta},\vec{\sigma})}{E^D(\vec{\delta},\vec{\sigma}_{max})}$
Power Gain (PG %)	$\frac{\varphi(\vec{\sigma}_{max})-\varphi^D(\vec{\sigma})}{\varphi(\vec{\sigma}_{max})}$

4.2.2 Evaluation on Different Green Metrics

Based on the idea of the above strategy, a bruce-force heuristic optimal energy algorithm, referred to as Opt_HOE, which adopts a fixed value as upper bound,i.e. $h_i = a\ target\ delay$, where $1 \leq i \leq K$, for per-node flow delay to obtain energy optimization, is analyzed through the two green metrics in TABLE 4.1.

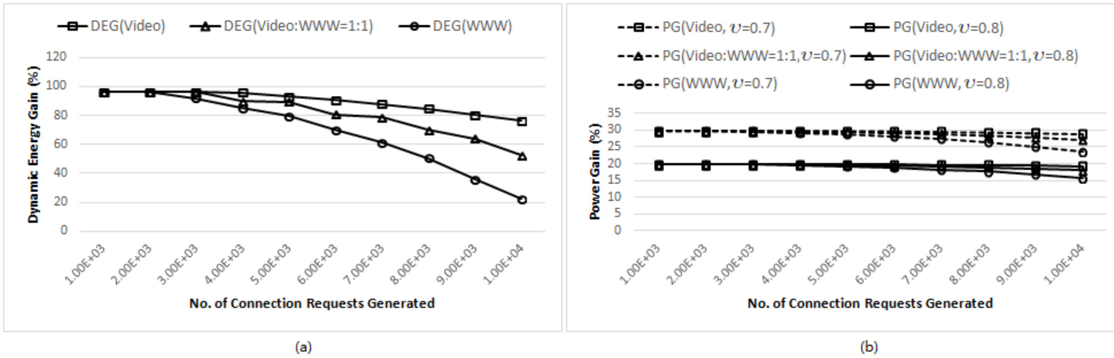

Figure 4.1: (a) Dynamic energy gains over agreeable delays and (b) Power Gains with $\upsilon = 0.7$& 0.8, under different class traffic for Opt_HOE.

Fig.4.1(a) depicts that the dynamic energy gains (DEGs) over agreeable delays of the supported traffic load from different class of sources. The results show that the bruce-force heuristic, Opt_HOE, is effective to save energy for the used network devices along the routing path, especially when the traffic load is not high. Under the given frequency range of $[50, 250]$ MHz, the dynamic energy saving over the agreeable delays can achieve up to 96% when the traffic load is very low, and as expected, the dynamic energy saving effectiveness decreases as the network load increases along the given path. Fig.4.1(b) shows that PGs, which considers both static power and dynamic power, has a similar curve trend as DEGs: with the increasing number of connection requests, the power saving decreases. It is worth noting that when the value of the static power ratio, υ, decreases, which means the proportion of dynamic power in the entire power consumption increases, it will lead to higher PGs. Take the traffic source of $1:1$ Video:WWW for example, under the given frequency range of $[f_{min}, f_{max}] = [50, 250]$ MHz, when $\upsilon_i = 0.8$, $1 \leq i \leq K$, the power saving can achieve up to 19.84%, while when $\upsilon_i = 0.7$, $1 \leq i \leq K$, the power saving can reach up to 29.76%.

4.2.3 Limitations and and Further Studies

In order to solve the energy optimization problem for wired networks, we first formally establish an energy consumption model based on agreeable delays of supported traffic flows in a give routing path. Then we propose a load-based, optimal energy strategy and analyze a bruce-force heuristic algorithm, which can be used to assign feasible per-node delay and execution speed values so that a specific objective of minimizing network energy consumption is achieved. A simulation framework is used to assess the performance of the proposed heuristic in terms of energy and power gains. Current simulation results show that the bruce-force heuristic is effective on energy saving for network devices along the given routing path, especially when the network load is not high. The limitation is that the current bruce-force heuristic algorithm, adopting the fixed values as the upper bounds of per-node delays, is less intelligent. In the coming work, we will further explore a methodology to dynamically compute or evaluate the upper bound values of the delay based on the current workload, and seek more intelligent heuristic algorithms to achieve the energy minimization, under QoS constrains.

5.0 EXPLORATIONS OF SLEEP-BASED POWER MANAGEMENT

In addition to DVFS-based energy- and QoS-aware strategies, another possible strategy to optimize the IP network consumption is represented by sleep-based, energy- and QoS-aware network management, which aims at adapting the whole network power consumption to the traffic levels by optimizing the network configuration and putting to sleep the redundant network elements, while taking into network performance requirements. This chapter will briefly discuss the explorations of sleep-based energy minimization, as future work.

5.1 BACKGROUND

Device sleeping represents the main potential source of saving because the consumption of current network devices is not proportional to the utilization level: so that, the overall network consumption is constantly close to maximum. As introduced in Chapter 2, the consumption of the base system is the major contributor to the overall energy consumption, switching off the whole router, therefore, could save more energy than only switching off the line cards. Despite its benefits, this technique of switching off the whole router raises several network degradation problems such as loss of connectivity or longer period to wake up. On the contrary, constantly switching network elements, such as line cards, off and on could be more energy consuming than keeping them on all the time. Currently, a large body of sleep-based, energy-aware strategies have been proposed.

Some researches choose to switch off individual line cards and remap the links to other ones. This avoids discontinuities and saves power when the traffic load is light. In [31], Fisher et al. propose an form of infrastructure sleeping where they shut down the redundant cables and the line cards, instead of the whole router, during periods of low utilization. In [36], routing reconfiguration at different layer, namely IP layer (the virtual layer) and WDM (the physical layer), for achieving energy saving through switching off line cards, is compared. The scheme that rerouters demands in the virtual layer achieves the best energy saving. Similarly, in [37], Shang et al. also propose a scheme to switch off line cards when traffic load is low. In [66], in order to improve the energy efficiency of backbone networks by dynamically adjusting the number of active links according to network load, Carpa et al. propose an intra-domain software-defined network (SDN) approach, an energy-aware traffic engineering technique, to select and turn off a subset of links. The implemented solution shows that as much as 44% of links can be switched off to save energy in real backbone networks. Recently, Virtualized Network Environment (VNE) has recently emerged as a solution to address the challenges of future Internet. It is essential to develop novel techniques to reduce VNEs energy consumption. In [67], Ghazisaeedi et al. propose a novel optimization algorithm for VNE, by sleeping reconfiguration on the maximum number of physical links during off-peak hours, while still guaranteeing the connectivity and off-peak bandwidth availability for supporting parallel virtual networks over the top. Simulation results based on the GANT network topology show this algorithm is able to put notable number of physical links to sleep during off-peak hours while still satisfying the bandwidth demands requested by ongoing traffic sessions in the virtual networks. It, however, does not change mapping of VNs, this decreases the level of energy saving. In [68], the same authors propose an energy saving method that optimizes VNEs energy consumption during the off-peak time. This method reconfigures mapping for some of the embedded virtual links in the off-peak period. The proposed strategy enables providers to adjust the level of the reconfiguration, and accordingly control probable traffic disruptions due to the reconfiguration. This problem is formulated as a Binary Integer Linear Program (BILP). the defined BILP is NP-hard, a novel heuristic algorithm is also suggested. The proposed energy saving methods are evaluated over random VNE scenarios. The results confirm the defined solutions are able to save notable amounts of energy during off-peak period, while still accommodating off-peak traffic demands of involved virtual networks.

Other researches, however, consider to put devices and their components into sleep when they are not used, to save more energy. In [69], authors propose an energy-aware traffic engineering solution to minimize the energy consumption of the network through a management strategy that selectively switches off devices according to the traffic level, and model a set of traffic scenarios corresponding to different time periods and consider a set of traffic scenarios and jointly optimize their energy consumption assuming a per-flow routing. In [38], Chiaraviglio et al. propose an algorithm that can selectively turn off some nodes and links of an IP-based backbone network during off-peak times. They demonstrated that an energy saving of at least 23% is possible for the total energy consumed by the backbone network. In [32], Chiaraviglio et al. model a network for minimizing the energy consumption by switching off idle nodes (routers) and idle links, witch subjects to flow conservation and maximum link utilization constraints. The problem is NP-hard, so in [25], several simple heuristic algorithms are employed, which sort all the nodes depending on the number of links, the amount of flows they accommodate, or use a random strategy to switch off for saving energy. In a simple network scenario, which includes core, edge, and aggregate networks, it is possible to switch off 30% of links and 50% of nodes. But most of them do not consider some practical problems of the on/on approach: switching on and off takes time, it leads to a network reconfiguration because of topology change, and a wake-up method is required to determine how and when nodes and links should be switched on again. Bianzino et al. extend their work by considering a real-world case in [35]. The problem for minimizing the number of nodes and links for saving energy, given a certain traffic demand, has been solved by Integer Problem Formulation (ILP) for simple networks. The algorithm switches off devices that consume more power in descending order. The results show that it is possible to reduce energy consumption by more than 23%, that is, 3 GWh/year in real network scenario.

5.2 FUTURE WORK

As discussed in the previous studies, potential higher energy saving can be achieved by sleep-based, energy-aware strategies. In recent years, the landscape of the Internet is fast changing with the introduction of streaming content such as video, high definition television and

Voice over IP (VoIP), with more stringent QoS requirements [70]. Given the ever increasing importance of the Internet, knowledge of its traffic has become increasingly critical. For instance, traffic properties are highly dependent on time scale, an long time scales (hours to days to weeks) traffic exhibits strong periodicities: there are distinct diurnal and weekly cycles with traffic peaks occurring around midday or in the evening and troughs in the early morning. This pattern correlates to user behaviour, where they access the Internet during the day for work or school and sleep in the night. Therefore, further studying the traffic measurement and prediction during peak and off-peak times, and seeking intelligent energy- and QoS-aware strategies to achieve energy minimization though using different sleep modes over different periods will be our further work, which will involve the following aspects:

1. study Internet traffic behavior and explore traffic estimation, prediction and provisioning in a IP network.
2. explore existing mechanisms of traffic matrix measurement and prediction which use different time scale, i.e. quarter-hour, hour, day and week.
3. further investigate SDN-based or VN-based, energy-aware traffic engineering in core networks.
4. build up a speed-based, energy optimization framework, taking into account the tradeoff between energy saving and QoS constraints, within which we can
   - create a generic and global network energy consumption model for a given IP network.
   - design a sleep-based, energy-aware strategy, which can smartly make decision to shutdown maximal number of network devices or components to minimize the energy consumption adapting to the traffic load.
   - propose various load-aware, optimal energy heuristic algorithms to achieve the energy minimization.
5. set up a simulation framework, which is used to assess the performance of the proposed heuristics in terms of energy and power gains.
6. define energy-efficient metrics

6.0 SUMMARY

The explored existing dynamic power-saving techniques and solutions are potential to save significant energy, they, however, have the increasing of network latency as a drawback. Speed scaling causes a stretching of packet service times because of slowing-down, while sleep mode introduces an additional delay due to wake-up times, these issues and challenges need to be overcome to enable solutions more eco-friendly and eco-sustainable. In order to improve environmental and economic sustainability, seeking intelligent strategies incorporating energy-awareness into network control and management become more and more critical for green Internet design. Based on the exploration of the current solutions and new research trends for future green wired networks, the conclusions indicate that researches on dynamic power management for next-generation wired networks should mainly address the following aspects: (i) effective energy-aware architecture design; (ii) energy management strategies to adapt the power consumption of networks to current traffic load; (iii) energy efficient metrics; (iv) fine balance the trade-offs between performance and energy.

Among current dynamic power management techniques, speed scaling enable to modulate energy absorption according to the actual workload through slowing down network components. While techniques based on sleep mode will help to further cut power consumption of unused devices (or parts of them) by shutting down network elements. These techniques may eventually impact on next-generation network devices by providing “energy-aware” profiles. Consequently, seeking intelligent energy-aware strategies to make optimal decisions to switch different power-saving modes by using these techniques, while taking into account the trade-off between energy saving and network performance, becomes our motivation of this work. Firstly, we explore and propose three families of DVFS-based, QoS-aware packet scheduling schemes, the best one can achieve up to 10% energy saving of the whole energy consumption in high-speed networks. In order to further explore dynamic power management based on speed scaling, we study how to formulate the energy optimization problem by using mathematical programming model, which combines DVFS technique with a given traffic scheduling policy. Current simulation results show that minimizing energy consumption can be achieved through DVFS-based, load-aware heuristic algorithms, without QoS violation. In addition, considering the potential higher energy saving by using sleep mode approaches compared to speed scaling ones, as future work, I will further explore sleep-based, energy-aware strategies, which are used to optimize energy by switching off network equipment when they are not used. The proposed work will be completed following the timeline shown in TABLE 6.1.

Table 6.1: Timeline of Proposed Work.

Date	**Content**	**Deliverable results**
Jan.	Finish DVFS-based energy optimization in Chapter 4	A paper for publication
Feb.	Explore sleep-based, energy-aware strategies	A sleep-based, energy-aware framework build-up
Mar.- Apr.	Study the problem of sleep-based power management	Analytical models and optimization problem formulation
May - Jun.	Finish Simulation and result analysis	A paper for publication
Jun. - July.	Thesis writing	Thesis ready for defense
Aug. - Sep.	Thesis revising	Completed thesis

BIBLIOGRAPHY

[1] J.-M. Pierson, *Large-scale Distributed Systems and Energy Efficiency: A Holistic View.* 111 River Street, Permissions Department, Hoboken, NJ 07030, USA: John Wiley & Sons, 2015.

[2] G.-Q. Zhang, G.-Q. Zhang, Q.-F. Yang, S.-Q. Cheng, and T. Zhou, "Evolution of the internet and its cores," *New Journal of Physics*, vol. 10, no. 12, p. 123027, 2008.

[3] J. Chabarek, J. Sommers, P. Barford, C. Estan, D. Tsiang, and S. Wright, "Power awareness in network design and routing," in *INFOCOM 2008. The 27th Conference on Computer Communications. IEEE*, 2008, pp. 1130–1138.

[4] C. Lubritto, A. Petraglia, C. Vetromile, F. Caterina, A. D'Onofrio, M. Logorelli, G. Marsico, and S. Curcuruto, "Telecommunication power systems: energy saving, renewable sources and environmental monitoring," in *INTELEC 2008-2008 IEEE 30th International Telecommunications Energy Conference.* IEEE, 2008, pp. 1–4.

[5] J. G. Koomey *et al.*, "Estimating total power consumption by servers in the us and the world," 2007.

[6] W. Vereecken, L. Deboosere, D. Colle, B. Vermeulen, M. Pickavet, B. Dhoedt, and P. Demeester, "Energy efficiency in telecommunication networks," in *Proceedings of NOC2008, the 13th European Conference on Networks and Optical Communications*, 2008, pp. 44–51.

[7] S. Lambert, W. Van Heddeghem, W. Vereecken, B. Lannoo, D. Colle, and M. Pickavet, "Worldwide electricity consumption of communication networks," *Optics express*, vol. 20, no. 26, pp. B513–B524, 2012.

[8] R. Bolla, R. Bruschi, A. Carrega, F. Davoli, D. Suino, C. Vassilakis, and A. Zafeiropoulos, "Cutting the energy bills of internet service providers and telecoms through power management: An impact analysis," *Computer Networks*, vol. 56, no. 10, pp. 2320–2342, 2012.

[9] C. Lange, D. Kosiankowski, C. Gerlach, F.-J. Westphal, and A. Gladisch, "Energy consumption of telecommunication networks," *ECOC 2009*, 2009.

[10] R. S. Tucker, R. Parthiban, J. Baliga, K. Hinton, R. W. Ayre, and W. V. Sorin, "Evolution of wdm optical ip networks: A cost and energy perspective," *Journal of Lightwave Technology*, vol. 27, no. 3, pp. 243–252, 2009.

[11] N. P. Group, "Nature photonics," in *Nature Photonics Technology Conference 2007.* Tokyo, Japan, 2007, pp. 1–8.

[12] C. Lange, D. Kosiankowski, R. Weidmann, and A. Gladisch, "Energy consumption of telecommunication networks and related improvement options," *Selected Topics in Quantum Electronics, IEEE Journal of*, vol. 17, no. 2, pp. 285–295, 2011.

[13] K. Hinton, J. Baliga, M. Feng, R. Ayre, and R. S. Tucker, "Power consumption and energy efficiency in the internet," *IEEE Network*, vol. 25, no. 2, pp. 6–12, 2011.

[14] R. Bolla, R. Bruschi, F. Davoli, and F. Cucchietti, "Energy efficiency in the future internet: a survey of

existing approaches and trends in energy-aware fixed network infrastructures," *Communications Surveys & Tutorials, IEEE*, vol. 13, no. 2, pp. 223–244, 2011.

[15] A. P. Bianzino, C. Chaudet, D. Rossi, and J.-L. Rougier, "A survey of green networking research," *Communications Surveys & Tutorials, IEEE*, vol. 14, no. 1, pp. 3–20, 2012.

[16] S. Zeadally, S. U. Khan, and N. Chilamkurti, "Energy-efficient networking: past, present, and future," *The Journal of Supercomputing*, vol. 62, no. 3, pp. 1093–1118, 2012.

[17] D. R. Recupero *et al.*, "Toward a green internet," *Science*, vol. 339, no. 6127, pp. 1533–1534, 2013.

[18] M. Mandviwalla and N.-F. Tzeng, "Energy-efficient scheme for multiprocessor-based router linecards," in *Applications and the Internet, 2006. SAINT 2006. International Symposium on.* IEEE, 2006, pp. 8–pp.

[19] G. L. Valentini, W. Lassonde, S. U. Khan, N. Min-Allah, S. A. Madani, J. Li, L. Zhang, L. Wang, N. Ghani, J. Kolodziej *et al.*, "An overview of energy efficiency techniques in cluster computing systems," *Cluster Computing*, vol. 16, no. 1, pp. 3–15, 2013.

[20] M. E. T. Gerards, "Algorithmic power management: Energy minimisation under real-time constraints," Ph.D. dissertation, Centre for Telematics and Information Technology, University of Twente, 2014.

[21] S. Nedevschi, L. Popa, G. Iannaccone, S. Ratnasamy, and D. Wetherall, "Reducing network energy consumption via sleeping and rate-adaptation," in *NSDI*, vol. 8, 2008, pp. 323–336.

[22] R. Bolla, F. Davoli, R. Bruschi, K. Christensen, F. Cucchietti, and S. Singh, "The potential impact of green technologies in next-generation wireline networks: Is there room for energy saving optimization?" *Communications Magazine, IEEE*, vol. 49, no. 8, pp. 80–86, 2011.

[23] B. Zhang, K. Sabhanatarajan, A. Gordon-Ross, and A. George, "Real-time performance analysis of adaptive link rate," in *Local Computer Networks, 2008. LCN 2008. 33rd IEEE Conference on.* IEEE, 2008, pp. 282–288.

[24] R. J. (2014) Energy efficient ethernet: Technology, application and why you should care. [Online]. Available: https://communities.intel.com/community/wired/blog/2011/05/05/

[25] L. Chiaraviglio, M. Mellia, and F. Neri, "Reducing power consumption in backbone networks," in *Communications, 2009. ICC'09. IEEE International Conference on.* IEEE, 2009, pp. 1–6.

[26] M. Alonso, J. M. Martinez, V. Santonja, and P. Lopez, "Reducing power consumption in interconnection networks by dynamically adjusting link width," in *Euro-Par 2004 Parallel Processing.* Springer, 2004, pp. 882–890.

[27] Cisco, "http://www.ici-cn.com/download/brochure/convergein *Converge IP and DWDM Layers in the Core Network. White paper*, 2007.

[28] J. Galan-Jimenez and A. Gazo-Cervero, "Elee: Energy levels-energy efficiency tradeoff in wired communication networks," *Communications Letters, IEEE*, vol. 17, no. 1, pp. 166–168, 2013.

[29] N. Vasić and D. Kostić, "Energy-aware traffic engineering," in *Proceedings of the 1st International Conference on Energy-Efficient Computing and Networking.* ACM, 2010, pp. 169–178.

[30] M. Gupta and S. Singh, "Greening of the internet," in *Proceedings of the 2003 conference on Applications, technologies, architectures, and protocols for computer communications.* ACM, 2003, pp. 19–26.

[31] W. Fisher, M. Suchara, and J. Rexford, "Greening backbone networks: reducing energy consumption by shutting off cables in bundled links," in *Proceedings of the first ACM SIGCOMM workshop on Green networking.* ACM, 2010, pp. 29–34.

[32] L. Chiaraviglio, M. Mellia, and F. Neri, "Energy-aware networks: Reducing power consumption by switching off network elements," in *FEDERICA-Phosphorus tutorial and workshop (TNC2008)*, 2008.

[33] M. Gupta and S. Singh, "Dynamic ethernet link shutdown for energy conservation on ethernet links," in *Communications, 2007. ICC'07. IEEE International Conference on.* IEEE, 2007, pp. 6156–6161.

[34] B. Nordman and K. Christensen, "Proxying: The next step in reducing it energy use," *Computer*, vol. 43, no. 1, pp. 91–93, 2010.

[35] A. P. Bianzino, C. Chaudet, F. Larroca, D. Rossi, and J.-L. Rougier, "Energy-aware routing: a reality check," in *GLOBECOM Workshops (GC Wkshps), 2010 IEEE.* IEEE, 2010, pp. 1422–1427.

[36] F. Idzikowski, S. Orlowski, C. Raack, H. Woesner, and A. Wolisz, "Saving energy in ip-over-wdm networks by switching off line cards in low-demand scenarios," in *Optical Network Design and Modeling (ONDM), 2010 14th Conference on.* IEEE, 2010, pp. 1–6.

[37] Y. Zhang, M. Tornatore, P. Chowdhury, and B. Mukherjee, "Time-aware energy conservation in ip-over-wdm networks," in *Photonics in Switching.* Optical Society of America, 2010, p. PTuB2.

[38] L. Chiaraviglio, M. Mellia, and F. Neri, "Energy-aware backbone networks: a case study," in *Communications Workshops, 2009. ICC Workshops 2009. IEEE International Conference on.* IEEE, 2009, pp. 1–5.

[39] K. Sabhanatarajan, A. Gordon-Ross, M. Oden, M. Navada, and A. George, "Smart-nics: Power proxying for reduced power consumption in network edge devices," in *Symposium on VLSI, 2008. ISVLSI'08. IEEE Computer Society Annual.* IEEE, 2008, pp. 75–80.

[40] Q. Yu, T. Znati, and W. Yang, "Energy-efficient, qos-aware packet scheduling in high-speed networks," *Selected Areas in Communications, IEEE Journal on*, vol. 33, no. 12, pp. 2789–2800, 2015.

[41] ——, "Energy-efficient, delay-aware packet scheduling in high-speed networks," in *Computing and Communications Conference (IPCCC), 2015 IEEE 34th International Performance.* IEEE, 2015, pp. 1–8.

[42] A. Vishwanath Member, K. Hinton, R. Ayre, and R. Tucker, "Modeling energy consumption in high-capacity routers and switches," *Selected Areas in Communications, IEEE Journal on*, vol. 32, no. 8, pp. 1524–1532, 2014.

[43] L. J. Wobker. (2012) Power consumption in high-end routing systems. [Online]. Available: https://www.nanog.org/meetings/nanog54/presentations/Wednesday/Wobker.pdf

[44] H. Imaizumi and H. Morikawa, "Directions towards future green internet," in *Towards Green Ict.* Niels Jernes Vej 10, 9220 Aalborg, Denmark: River Publishers, 2010, vol. 9, pp. 37–53.

[45] R. Bolla, R. Bruschi, A. Cianfrani, and M. Listanti, "Enabling backbone networks to sleep," *Network, IEEE*, vol. 25, no. 2, pp. 26–31, 2011.

[46] C. Gunaratne, K. Christensen, and B. Nordman, "Managing energy consumption costs in desktop pcs and lan switches with proxying, split tcp connections, and scaling of link speed," *International Journal of Network Management*, vol. 15, no. 5, pp. 297–310, 2005.

[47] C. Vassilakis, "Towards energy efficient internet service providers econet perspective," in *GN3 Green Networking Workshop: Advances in Environmental Policy and Practice, Utrecht, Netherlands*, 2012.

[48] X. Chen, X. Liu, S. Wang, and X.-W. Chang, "Tailcon: Power-minimizing tail percentile control of response time in server clusters." in *SRDS*, 2012, pp. 61–70.

[49] D. Hayes, D. Ros, L. Andrew, and S. Floyd. (2014) Common tcp evaluation suite. [Online]. Available: https://tools.ietf.org/html/draft-irtf-iccrg-tcpeval-01

[50] E. Jonckheere, K. Shah, and S. Bohacek, "Dynamic modeling of internet traffic for intrusion detection," in *American Control Conference, 2002. Proceedings of the 2002*, vol. 3. IEEE, 2002, pp. 2436–2442.

[51] K. Shah, S. Bohacek, and E. A. Jonckheere, "On the predictability of data network traffic," in *Proceedings of the American Control Conference*, vol. 2, 2003, pp. 1619–1624.

[52] Z. Móczár, S. Molnar, and B. Sonkoly, "Multi-platform performance evaluation of digital fountain based transport," in *Science and Information Conference (SAI), 2014*. IEEE, 2014, pp. 690–697.

[53] Intel. (2012) Data plane development kit overview. [Online]. Available: http://www.intel.com/content/dam/www/public/us/en/documents/presentation/dpdk-packet-processing-ia-overview-presentation.pdf

[54] W. Simpson, *Video over IP: a practical guide to technology and applications.* Taylor & Francis, 2006.

[55] http://www.voip-info.org/wiki/view/Codecs.

[56] T. Szigeti and C. Hattingh, *End-to-end qos network design.* 800 East 96th Street, Indianapolis, Indiana 46240, USA: Cisco press, 2005.

[57] ITU-T, "Recommendation g. 114," *One-Way Transmission Time, Standard G*, vol. 114, 2003.

[58] J. Ellis, C. Pursell, and J. Rahman, *Voice, video, and data network convergence: architecture and design, from VoIP to wireless.* Academic Press, 2003.

[59] A.-C. Orgerie, M. D. d. Assuncao, and L. Lefevre, "A survey on techniques for improving the energy efficiency of large-scale distributed systems," *ACM Computing Surveys (CSUR)*, vol. 46, no. 4, p. 47, 2014.

[60] X. Cui, B. N. Mills, T. Znati, and R. G. Melhem, "Shadows on the cloud: An energy-aware, profit maximizing resilience framework for cloud computing." in *CLOSER*, 2014, pp. 15–26.

[61] C. L. Liu and J. W. Layland, "Scheduling algorithms for multiprogramming in a hard-real-time environment," *Journal of the ACM (JACM)*, vol. 20, no. 1, pp. 46–61, 1973.

[62] T. F. Znati and R. Melhem, "Node delay assignment strategies to support end-to-end delay requirements in heterogeneous networks," *Networking, IEEE/ACM Transactions on*, vol. 12, no. 5, pp. 879–892, 2004.

[63] B. Field, T. F. Znati, and D. Mosse, "V-net: A framework for a versatile network architecture to support real-time communication performance guarantees," in *INFOCOM'95. Fourteenth Annual Joint Conference of the IEEE Computer and Communications Societies. Bringing Information to People. Proceedings. IEEE.* IEEE, 1995, pp. 1188–1196.

[64] A. Vishwanath, K. Hinton, R. Ayre, and R. Tucker, "Modelling energy consumption in high-capacity routers and switches," 2014.

[65] (2006) Csp series. [Online]. Available: http://pdf.datasheet.online/datasheets-1/raltron_electronics/CSPAVI-FREQ.pdf

[66] R. Carpa, O. Gluck, L. Lefevre, and J.-C. Mignot, "Improving the energy efficiency of software-defined backbone networks," *Photonic Network Communications*, vol. 30, no. 3, pp. 337–347, 2015.

[67] E. Ghazisaeedi, N. Wang, and R. Tafazolli, "Chapter5:link sleeping optimization for green virtual network infrastructures," in *2012 IEEE Globecom Workshops.* IEEE, 2012, pp. 842–846.

[68] E. Ghazisaeedi and C. Huang, "Energy-efficient virtual link reconfiguration for off-peak time," in *2015 IEEE Global Communications Conference (GLOBECOM).* IEEE, 2015, pp. 1–7.

[69] L. G. Gianoli, "Energy-aware traffic engineering for wired ip networks," 2014.

[70] P. Tune and M. Roughan, "Internet traffic matrices: A primer," *Recent Advances in Networking*, vol. 1, 2013.