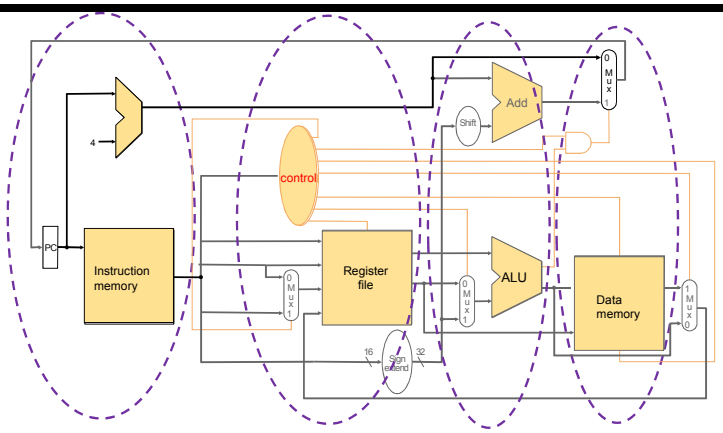
Where is the delay?



1) Instruction fetch

2) Decode and register read

3) ALU (compute)

4) Use memory

5) Register write

Candidate for a 5-stage pipeline

An analogous example: car wash

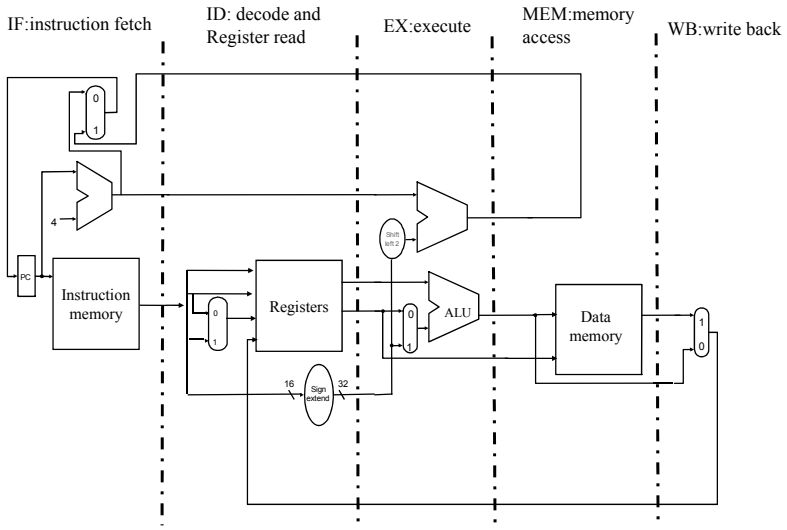
The non-pipelined car wash:

Soak
Bruch
Rinse
Dry

The pipelined car wash:

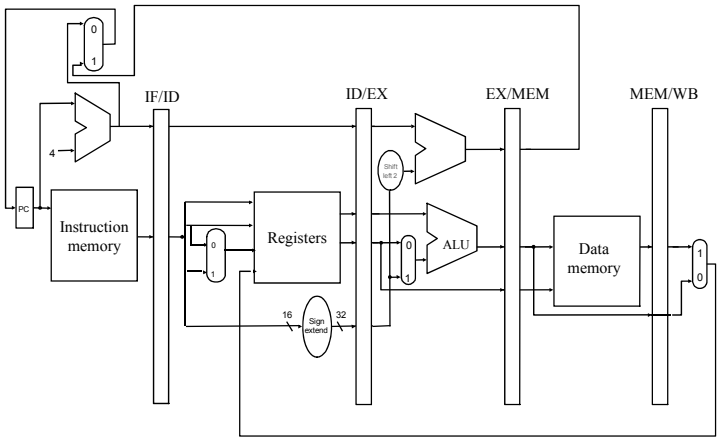
Soak | Bruch | Rinse | Dry

Basic Idea of a MIPS pipeline



What do we need to add to actually split the datapath into stages?

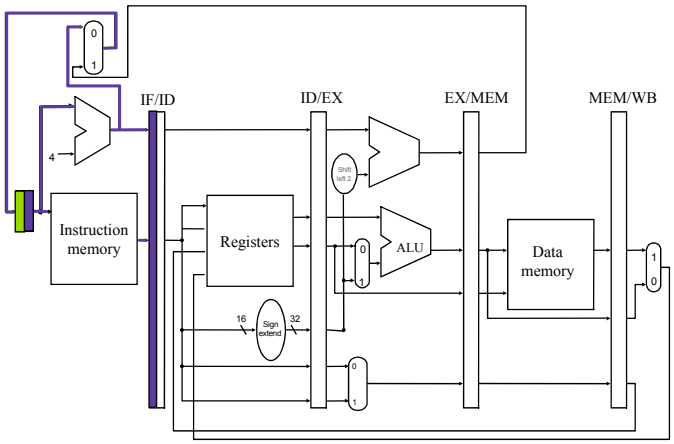
Inter-stage buffers



- Add buffers between consecutive stages (store data at the end of a clock cycle, and use it at the beginning of the next cycle)
- The cycle time should be long enough to allow the signals in each stage to propagate from the input to the output buffers of the stage

Pipelined execution of an instruction

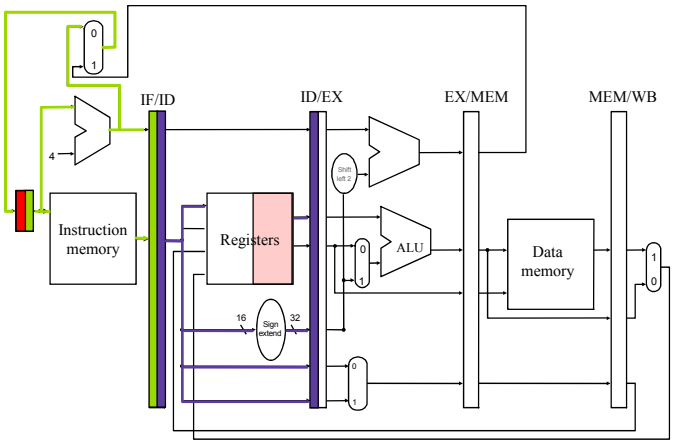
Cycle 1



lw

Pipelined execution of consecutive instructions

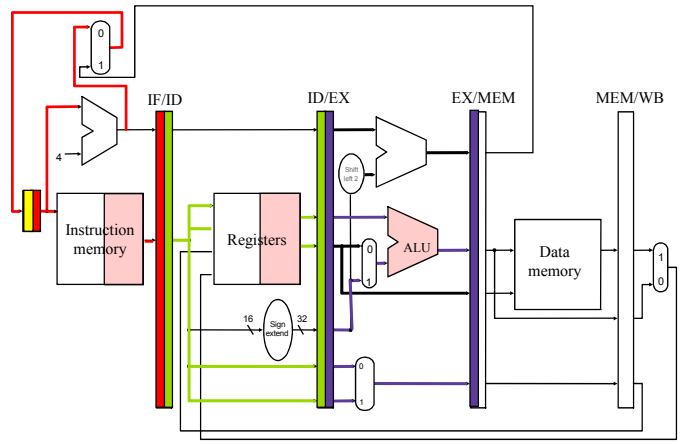
Cycle 2



add lw

Pipelined execution of consecutive instructions

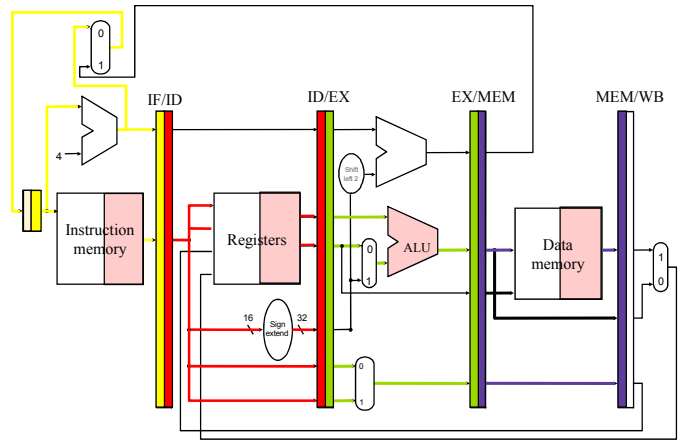
Cycle 3



sw add lw

Pipelined execution of consecutive instructions

Cycle 4



beq sw add lw