

Question 1:

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In this question, consider the following series of word addresses:

20, 33, 21, 4, 17, 33, 4

Assuming a direct mapped cache with 16 one-word blocks, show the content of the cache after each memory reference and indicate whether it is a hit or a miss. Use [tag, M(address)] to describe the content of each entry. For example [4, M(46)] indicates that the entry contains tag=4 and the data from memory location 46. Indicate that an entry E1 is replaced by E2 by crossing E1 and writing E2 next to it.

$$\begin{aligned} w / 16 & \quad w \bmod 16 \\ 20 &= 16 * 1 + 4 \\ 33 &= 16 * 2 + 1 \\ 21 &= 16 * 1 + 5 \\ 4 &= 16 * 0 + 4 \\ 17 &= 16 * 1 + 1 \end{aligned}$$

20(M), 33(M), 21(M), 4(M), 17(M), 33(M), 4(H)

0	
1	[2, M(33)] [1, M(17)] [2, M(33)]
2	
3	
4	[1, M(20)] [0, M(4)]
5	[1, M(21)]
6	
7	
8	
9	
10	
11	
12	
13	
14	
15	

index

Question 2:

7

In this question, consider the following series of word addresses:

20, 23, 21, 4, 21, 28, 22, 23, 5

Assuming a direct mapped cache with two-word blocks and total size of 16 words, show the content of the cache after each memory reference and indicate whether it is a hit or a miss. Use [4, M(46), M(47)] to indicate that the entry contains a block of two words from memory locations 46 and 47.

$$\begin{aligned} w & \quad B & B / 8 & B \bmod 8 \\ \text{word 20} &= \text{block 10} = 8 * 1 + 2 \\ \text{word 23} &= \text{block 11} = 8 * 1 + 3 \\ \text{word 21} &= \text{block 10} = 8 * 1 + 2 \\ \text{word 4} &= \text{block 2} = 8 * 0 + 2 \\ \text{word 28} &= \text{block 14} = 8 * 1 + 6 \\ \text{word 22} &= \text{block 10} = 8 * 1 + 2 \\ \text{word 5} &= \text{block 2} = 8 * 0 + 2 \end{aligned}$$

Notes:

$$B = w / 2$$

$$\text{Tag} = B / 8 = w / 16$$

$$\text{Index} = B \bmod 8 = (w \bmod 16) / 2$$

0	
1	
2	[1, M(20), M(21)] [0, M(4), M(5)] [1, M(20), M(21)] [0, M(4), M(5)]
3	[1, M(22), M(23)]
4	
5	
6	[1, M(28), M(29)]
7	

Block index

20(M), 23(M), 21(H), 4(M), 21(M), 28(M), 22(H), 23(H), 5(M)

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Question 3:

Compute the total number of bits required to implement a 512KB direct mapped cache with 4-bytes block size. Assume that each memory word is 32-bit long and the memory is byte addressable with 32-bits addresses. Note that the number of bits needed to implement the cache represents the total amount of memory needed for storing all of the data, tags and valid bits (ignore any other bits).

Cache size	512KB
Block size	one word
# of bits for data array	4096 Kbits
# of bits for tag array	1664 Kbits
# of bits for valid bits	128 Kbits
Total # of bits	5888 Kbits

$$\text{Cache Size: } 512\text{KB} = 2^{19} \text{ bytes}$$

$$\text{Block Size: } 2^0 \text{ word} = 2^2 \text{ bytes}$$

$$\# \text{ of blocks: } (2^{19})/(2^2) = 2^{17}$$

$$\text{Tag field: } (32-2-17) = 13 \text{ bits}$$

$$\# \text{ of bits for data array} = 512 * 8 = 4096 \text{ Kbits}$$

$$\# \text{ of bits for tag array} = 2^{17} * 13 = 1664 \text{ Kbits}$$

$$\# \text{ of bits for valid bits} = 2^{17} * 1 = 128 \text{ Kbits}$$

$$\text{Total \# of bits} = 5888 \text{ Kbits}$$

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Question 4:

Compute the total number of bits required to implement a 512KB direct mapped cache with 16-bytes block size (4 words). Assume that each memory word is 32-bit long and the memory is byte addressable with 32-bits addresses. Note that the number of bits needed to implement the cache represents the total amount of memory needed for storing all of the data, tags and valid bits (ignore any other bits).

Cache size	512KB
Block size	one word
# of bits for data array	4096 Kbits
# of bits for tag array	416 Kbits
# of bits for valid bits	32 Kbits
Total # of bits	4544 Kbits

$$\text{Cache Size: } 512\text{KB} = 2^{19} \text{ bytes}$$

$$\text{Block Size: } 2^2 \text{ word} = 2^4 \text{ bytes}$$

$$\# \text{ of blocks: } (2^{19})/(2^4) = 2^{15}$$

$$\text{Tag field: } (32-4-15) = 13 \text{ bits}$$

$$\# \text{ of bits for data array} = 512 * 8 = 4096 \text{ Kbits}$$

$$\# \text{ of bits for tag array} = 2^{15} * 13 = 416 \text{ Kbits}$$

$$\# \text{ of bits for valid bits} = 2^{15} * 1 = 32 \text{ Kbits}$$

$$\text{Total \# of bits} = 4544 \text{ Kbits}$$