Lei Zhao

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Education

- **University of Pittsburgh** — Pittsburgh, PA, U.S.
  Ph.D. candidate of Computer Science — *Aug. 2014 – July. 2021 (expected)*
- **Northwestern Polytechnical University** — Xi'an, China
  Master of Computer Science — *Aug. 2011 – Apr. 2014*
- **Northwestern Polytechnical University** — Xi'an, China
  Bachelor of Software Engineering — *Aug. 2007 – July. 2011*

Selected Publications

- **SCA: A Secure CNN Accelerator for both Training and Inference**
  Lei Zhao, Youtao Zhang, and Jun Yang
  Design Automation Conference (DAC), 2020
- **RFAcc: A 3D ReRAM Associative Array based Random Forest Accelerator**
  Lei Zhao, Quang Deng, Youtao Zhang, and Jun Yang
  International Conference on Supercomputing (ICS), 2019
- **AEP: An Error-bearing Neural Network Accelerator for Energy Efficiency and Model Protection**
  Lei Zhao, Youtao Zhang, and Jun Yang
  International Conference On Computer Aided Design (ICCAD), 2017
- **Constructing Fast and Energy Efficient 1TnR based ReRAM Crossbar Memory**
  Lei Zhao, Lei Jiang, Youtao Zhang, Nong Xiao, and Jun Yang
  International Symposium on Quality Electronic Design (ISQED), 2017

Patents

- **System and method of deploying an artificial neural network on a target device**
  Youtao Zhang, **Lei Zhao**, and Jun Yang
  U.S. Patent, US20190147344A1

Research Projects

- **Machine Learning Accelerators** — Apr 2017 - Present
  Designer and Conductor
  - **Description**: Design ASIC accelerators based on existing or emerging memory technologies to improve performance and energy efficiency of machine learning computations with a focus on model security and user privacy.
  - **Achievements**: Three papers in [ICCAD'2017] [ICS'2019] [DAC'2020] and one U.S. patent.
- **Privacy-Preserving Medical Data Analysis** — Aug 2017 - Present
  Research Assistant
  - **Description**: Evaluate Neural Networks on medical data with homomorphic encryption to protect patient's private information.
  - **Achievements**: One paper to appear in ACM Transactions on Internet Technology (TOIT)
- **Emerging Memory Design** — Sept 2014 - Apr 2016
  Designer and Conductor
  - **Description**: Emerging non-volatile memories (NVM) (e.g. DWM, SSTMRAM, ReRAM) are the future of Process-in-Memory (PIM) architectures for machine learning acceleration, especially neural networks. This project targets the challenges of circuit level optimization of NVM for machine learning acceleration.
  - **Achievements**: Four papers in [ICCD'2015] [ISQED'2017] [NVMSA'2017] [ICCAD'2017]

Skills

- **Computer Architecture**: Emerging Memory Technologies, Accelerator Design
- **Machine Learning**: Neural Networks, Computer Vision, Natural Language Processing
- **Languages**: Chinese (Native), English (Proficient)