0. Goals and Course Description

In this course, we study the hardware structure of computer systems and subsystems. Topics include: pipelined processor architecture, cache and main memory organization, I/O processing and storage, basic interconnection structures in multiprocessor systems, and graphics processor architectures. Students will write programs to gain insight about how user programs perform on modern computer architectures.

1. Textbook and Course Materials

   Other course materials will be distributed via course web page (www.cs.pitt.edu/~cho/cs1541/).

2. Instructor

   Sangyeun Cho (cho@cs.pitt.edu, 412-383-7018)
   Office hours: Monday/Wednesday 8:00am ~ 10:00am @SENSQ 5415 or by appointment

3. TA

   Yu Du (fisherdu@cs.pitt.edu, 412-624-9955)
   Office hours: Tuesday/Thursday 4:00pm ~ 6:00pm @SENSQ 6504

4. Class Hours and Classroom

   Lecture: Monday/Wednesday 10:00am ~ 11:15am @SENSQ 5129
5. Student Evaluation

Homework (problem set, programming, etc.) 50%
Mid-term exams 20%
Final exam 30%

6. Other Policies

- Late submissions of assignment will NOT be accepted.
- Plagiarism and cheating are strictly prohibited. Each student is expected to do his/her own work. Offense of this rule will result in a “0” in a particular assignment or exam. The second offense will lead to an automatic “F” for the course and the offender may be subject to stronger actions.
- Students are expected to be present for all exams. Make-up exams will only be given in the event of an emergency and only if the instructor is informed in advance.

7. Students with disabilities

If you have a disability for which you are or may be requesting an accommodation, you are encouraged to contact both your instructor and the Office of Disability Resources and Services (DRS), 140 William Pitt Union, 412-648-7890/412-383-7355 (TTY), as early as possible in the term. DRS will verify your disability and determine reasonable accommodation for this course.