Assignment

1. We want to compare the maximum bandwidth for a synchronous and an asynchronous bus. The synchronous bus has a clock cycle time of 30 ns and each bus transmission takes one clock cycle. The asynchronous bus requires 20 ns per handshake. The data portion of both buses is 16 bits wide. Find the bandwidth for each bus when performing one-word reads from a 100 ns memory.

2. Assume that the number of clock cycles for a polling operation -- including transferring to the polling routine, accessing the device and restarting the user program, is 200 and that the processor executes with a 1GHz clock. Determine the fraction of CPU time consumed for a hard drive, assuming that the devices are potentially always busy and you poll often enough so that no data is ever lost. It is given that the hard disk transfers data in 4-word chunks and can transfer at 8 MB per sec. If we have the same processor and hard drive as discussed above, but we are using an interrupt driven IO and the overhead for each transfer, including the interrupt, is 300 clock cycles, find the fraction of the processor consumed if the hard drive is only transferring data 5% of the time.

3. Suppose that we have the same processor and hard drive as in the previous question. Assume that the initial setup of a DMA transfer takes 1000 clock cycles for the processor, and assume that the handling of the interrupt at DMA completion requires 400 clock cycles for the processor. The hard drive transfers at the rate of 8 MB per sec and uses DMA. If the average transfer from the disk is 16 KB, what fraction of the processor time is consumed if the disk is actively transferring 100% of the time? Ignore any impact from bus contention between the processor and DMA controller.

4. For this question, assume you have arrays X and W, and an integer scalar variable k. Here is the code snippet for parts (a) and (b) below.

```c
for (j = 0; j < 10; j++)
    for (i = 0; i < 10; i++)
        X[i] = X[i+1] * W[j] + k;
```

Assume that the body of the loop itself can not be parallelized. However, each iteration of the loop may be executed on different processors (if dependences permit).

(a) Assuming that the data arrays X and W and the scalar integer k are shared by all processors, can you get any speedup by running the loop on a SMP with 100 processors? Why or why not? Show a picture that demonstrates whether there are any dependences between the first four loop iterations (j=0 and i=0, 1, 2, 3)
(b) What can you do to the data arrays to improve the loop’s speedup on a multiprocessor? Show your changes to the loop. What is the maximum speedup that you can get with a 100 processor machine? Justify your answer.

5. Suppose we have a shared memory multiprocessor with two processors, P1 and P2. Further assume that this machine uses a 3-state snoopy cache coherence protocol. Addresses A1 and A2 map to the same cache line, but are different addresses. For the following sequence of memory operations, show the state of each cache line in each processor.

- Processor P1 reads address A1
- Processor P2 reads address A2
- Processor P1 writes “10” to address A2
- Processor P2 reads address A1
- Processor P2 reads address A2
- Processor P2 writes “20” to address A2