Assignment

1. You are designing the memory system for the 32-bit Steeler processor. Let’s suppose that the CPU architect designed the Steeler to have a base CPI of 1 (i.e., it’s an in-order single-issue processor) and a clock rate of 1 GHz. It’s known from experiments that 1 in 5 instructions executed by the Steeler is a load or store. Because the Steeler is a RISC design, no other instructions reference memory.

Your initial memory design is the following: a single level cache hierarchy with separate instruction and data caches, a main memory access latency of 20 n.sec., main memory and bus data width of 128 bits, a 32 byte cache line size, and a synchronous memory bus running at 200 MHz. Your instruction cache design is fantastic and achieves an instruction cache hit rate of 100% (good job, pat yourself on the back!).

But you’re worried that the misses from the data cache might saturate the bus. What is the minimum data cache miss rate that saturates the bus? To simplify the problem, assume the processor does not block on a cache miss.

2. For this question, assume the following bus characteristics.

- Synchronous processor-memory bus running at 100 MHz
- Data width of 64 bits
- Address and data are multiplexed on the same wires
- Each bus transmission takes 1 cycle
- The memory has a 100 n.sec. access latency

What is the peak bandwidth for this memory system?

3. Assume that the number of clock cycles for a polling operation -- including transferring to the polling routine, accessing the device and restarting the user program, is 200 and that the processor executes with a 1GHz clock. Determine the fraction of CPU time consumed for a hard drive, assuming that the devices are potentially always busy and you poll often enough so that no data is ever lost. It is given that the hard disk transfers data in 4-word chunks and can transfer at 8 MB per sec. If we have the same processor and hard drive as discussed above, but we are using an interrupt driven IO and the overhead for each transfer, including the interrupt, is 300 clock cycles, find the fraction of the processor consumed if the hard drive is only transferring data 5% of the time.
4. Suppose that we have the same processor and hard drive as in the previous question. Assume that the initial setup of a DMA transfer takes 1000 clock cycles for the processor, and assume that the handling of the interrupt at DMA completion requires 400 clock cycles for the processor. The hard drive transfers at the rate of 8 MB per sec and uses DMA. If the average transfer from the disk is 16 KB, what fraction of the processor time is consumed if the disk is actively transferring 100\% of the time? Ignore any impact from bus contention between the processor and DMA controller.

5. Let’s say we have a hard disk with the following characteristics:

- Capacity 9 GB
- Rotational speed 6000 RPM
- Average seek time 9 m.sec
- Sector size 256 bytes
- Controller latency overhead 2.3 m.sec
- Average access latency 16.4 m.sec

What is the average data transfer rate of this disk?