Assignment

(1)

Here is a series of references given as word addresses:

1, 5, 3, 8, 14, 18, 25, 37, 56, 43, 7, 4, 13, 27, 53, 5.

Assuming a direct-mapped cache with 16 one-word blocks that is initially empty, label each reference in the list as a hit or a miss and show the final contents of the cache.

(2)

Suppose a processor with a 16-word block size has an effective miss rate per instruction of 0.4%. Assume that the CPI without cache misses is 1.5. Consider the memories described in Figure 7.13 on page 561 in the textbook.

Suppose that the miss penalties for

- One-word-wide (narrow) memory organization is 150 clock cycles
- Wide memory organization is 50 clock cycles and
- Interleaved memory organization is 60 clock cycles

How much faster (or slower) is this processor when using the Wide memory than when using narrow or interleaved memories?

(3)

Suppose a computer's address size is 64 bits (using byte addressing), the cache size is 32 Kbytes (1 K = 2^10 bytes), the block size is 32 bytes and the cache is 4-way set-associative. Compute the following quantities are:

(a) the number of sets in the cache

(b) the number of index bits

(c) the number of tag address bits in a block
Consider three machines with different cache configurations:

**Cache1**: Direct mapped with one-word blocks

**Cache2**: Direct mapped with 8 word blocks

**Cache3**: Two-way set associative with 8 word blocks

For these machines, one half of the instructions contain a data reference. Assume that the cache miss penalty is $8 + \text{Block size in words}$. The CPI for this workload was measured on a machine with Cache1 and was found to be 2.0.

Which machine spends the most cycles on cache misses?