Extending the Lifetime of New Generation Memory Technologies
Santiago Bock, Alexandre Ferreira, Dr. Bruce Childers, Dr. Rami Melhem and Dr. Daniel Mossé
Department of Computer Science

1. Introduction
- Main memory is currently built with DRAM, which is a type of volatile memory.
- DRAM memories face two challenges: energy consumption (they need power to maintain stored information) and scalability (it is hard to build small capacitors).
- Phase Change Memory (PCM), a non-volatile memory, addresses this issues, but introduces other problems.
- PCM memories have a limit on the number of times that data can be written before the memory wears out.
- Most bits in PCM endure 10^9 writes, but some endure only 10^6 or 10^7 writes (weak bits) due to process variation.

2. Motivation
- The information stored inside memories is sometimes corrupted due to soft errors, which alter the contents of individual bits of memory.
- Error Correcting Codes (ECC) store redundant information along with the actual data to deal with soft errors.
- Soft errors do not affect PCM, but ECC is still used to improve endurance.
- ECC extends the lifetime of PCM memories by correcting errors caused by weak bits.
- Using the same extra capacity, can we get a higher lifetime than ECC?

3. Sparing
- Internally, memories are collections of bits organized in words, rows and pages (for example, 64 bits form a word, 32 words form a row and 32 rows form a page).
- ECC is typically applied to each word (for example, there could be 8 ECC bits per each 64-bit word).
- Instead of using these extra ECC bits, we can combine the ECC bits of different words to form spare words or rows.

4. Modeling Memory Lifetime
- We assume that weak bits are uniformly distributed across the memory.
- We calculate the probability that the lifetime of a word, row, page and of the whole memory is determined by the lifetime of the weak bits.
- Some definitions:
  - D: number of data bits per word
  - E: number of ECC bits per word
  - W: number of words per row
  - R: number of rows per page
  - SR: number of spare rows per page
  - P: number of pages in memory
  - p: fractions of weak bits
  - SW: number of spare words per row
  - q: probability of weak word with or without ECC
  - q_noECC: P(weak word no ECC) = \(1 - (1 - p)^{W} - (D + E)q(1 - p)^{W+E-1}\)
  - P(weak word ecc) = \(1 - (1 - p)^{D}\)
  - r: probability of weak row
  - P(weak row) = \(1 - \sum_{i=0}^{W} \binom{W}{i} (1 - p)^{W-i}(1 - q)^i\)
  - t: probability of weak page
  - P(weak page) = \(1 - \sum_{i=0}^{W} \binom{W}{i} (1 - p)^{W-i}(1 - q)^R\)
  - Probability of weak memory
  - P(weak memory) = \(1 - (1 - t)^P\)

5. Results
- Strong memories have a probability of being weak close to 0.
- Sparing yields strong memories for a larger range of fraction of weak bits than ECC.

6. Conclusions
- We proposed a sparing scheme to extend the lifetime of PCM memories.
- We developed a model to calculate the probability that a memory is weak, based on the fraction of weak bits in the memory.
- Using this model, we showed that sparing yields strong memories for a larger range of fraction of weak bits using the same extra capacity as ECC.
- We showed that sparing yields memories with lifetimes 44.2% higher than ECC.
- Using this model, we showed that sparing yields strong memories for a given value of probability.
- Sparing yields a lifetime of 6.57x10^7 with probability 99.9%, while ECC yields a lifetime of 4.56x10^6 with the same probability.