## CS1541 Fall 2008

Solution to the optional homework on Virtual Memory

## Question 1

Suppose that a virtual memory system has the following properties:
40-bit virtual byte address;
16KB pages;
32-bit physical address;
TLB has 8 entries and fully associative;
Valid, protection, dirty and use bits take a total of 4 bits (both TLB and page table have these).
Compute the following quantities:
(a) The total size (in bits) of TLB.

Answer:

Each TLB entry has: Valid Bit, Protection Bit, Dirty Bit, Use Bit, Tag Address (which is Virtual Page \#), and Physical Page \#.

Page Offset Length $=14$ (as the page size is 16 KB and $2 \wedge 14=16 \mathrm{~K}$ ).
Physical Page \# Length = Physical Address Length - Page Offset Length = 32 - 14 = 18
Virtual Page \# Length $==$ Virtual Address Length - Page Offset Length $=40-14=26$
TLB Entry Size $=4+26+18=48$
TLB Size $=$ \# TLB Entries * TLB Entry Size $=8 * 48=\underline{384 \text { bits }}=\underline{48 B}$.
(b) The total size (in bits) of the page table.

Answer:
Each PTE has: Valid Bit, Protection Bit, Dirty Bit, Use Bit, and Physical Page \#.

```
PTE Size = 4 + 18=22
# PTEs = 2^26
Page Table Size = # PTEs * PTE Size = 22 * 2^26 bits = \underline{176 MB}
```


## Question 2

Suppose that one computer has a virtual memory system as the following:
16-bit virtual address (byte addressing);
8 KB pages;
16-bit physical address (byte addressing);
TLB has 3 entries and fully associative;
TLB entry has four parts: valid bit, dirty bit, VPN (also called tag), PPN;
Page Table entry has three parts: valid bit, dirty bit, PPN;
LRU page replacement and TLB entry replacement.
Operating system on this computer allocates only 4 contiguous pages of the main memory to process A. The first page's address starts at $0 \times 4000$.

There are a series of virtual memory references of process A below. Indicate each reference causes TLB hit or TLB miss and show the contents of the TLB after each reference; indicate each reference causes Page Fault or not and show the contents of the Page Table after each reference. Initially, all entries in the TLB and Page Table are empty. Pure page-demanding is implemented, which means that a page is loaded into the memory only when accessed. Hard disk address of a physical page is not filled into page table.

| 0xA1F4 | Read |
| :--- | :--- |
| 0xFEA6 | Read |
| 0xE208 | Write |
| 0x2020 | Read |
| 0xB03E | Write |
| 0xD021 | Write |
| 0x689A | Read |
| 0x345C | Write |
| 0xCFDC | Write |
| 0x7ED2 | Write |
| 0x8038 | Read |

[^0]
## Answer (not complete):

Page Size $=8 \mathrm{~KB}=>$ Page Offset $=13$ bits.
Virtual Address Space $=16$ bits $=>$ High 3 bits are VPN.
Physical Address Space = 16 bits => PPN has 3 bits.
Process A has been allocated 4 contiguous physical pages starting at $0 \times 4000$ and $0 x 4000=0100000000000000=>$ The four physical pages' PPN are: 2, 3, 4, 5 .

Approach:

1. TLB Hit => if the reference is write, set "Dirty Bit" for the corresponding TLB entry to 1 .
2. TLB Miss:
a. TLB Operations

Find the replacement TLB entry; if that entry’s "Dirty Bit" is 1, set the "Dirty Bit" in the Page Table’s corresponding entry to 1.
b. Page Table Operations
(a) Page Table Hit $=>$ bring that entry to TLB.
(b) Page Table Miss (Page Fault) => find the replacement page via LRU, bring that PPN to the corresponding VPN
entry then
bring that entry to TLB; and empty the replaced Page Table entry (the corresponding VPN entry).
TLB

| Reference (virtual address) | Read/ Write | Left Most Four Bits | Hit/ Miss | Entry 0 |  |  |  | Entry 1 |  |  |  | Entry 2 |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | V | D | VPN | PPN | V | D | VPN | PPN | V | D | VPN | PPN |
| 0xA1F4 | R | 1010 | M | 1 | 0 | 5 | 2 | 0 |  |  |  | 0 |  |  |  |
| 0xFEA6 | R | 1111 | M | 1 | 0 | 5 | 2 | 1 | 0 | 7 | 3 | 0 |  |  |  |
| 0xE208 | W | 1110 | H | 1 | 0 | 5 | 2 | 1 | 1 | 7 | 3 | 0 |  |  |  |
| 0x2020 | R | 0010 | M | 1 | 0 | 5 | 2 | 1 | 1 | 7 | 3 | 1 | 0 | 1 | 4 |
| 0xB03E | W | 1011 | H | 1 | 1 | 5 | 2 | 1 | 1 | 7 | 3 | 1 | 0 | 1 | 4 |
| 0xD021 | W | 1101 | M | 1 | 1 | 5 | 2 | 1 | 1 | 6 | 5 | 1 | 0 | 1 | 4 |
| 0x689A | R | 0110 | M | 1 | 1 | 5 | 2 | 1 | 1 | 6 | 5 | 1 | 0 | 3 | 3 |
| 0x345C | W | 0011 | M | 1 | 1 | 1 | 4 | 1 | 1 | 6 | 5 | 1 | 0 | 3 | 3 |
| 0xCFDC | W | 1100 | H | 1 | 1 | 1 | 4 | 1 | 1 | 6 | 5 | 1 | 0 | 3 | 3 |
| 0x7ED2 | W | 0111 | H | 1 | 1 | 1 | 4 | 1 | 1 | 6 | 5 | 1 | 1 | 3 | 3 |
| 0x8038 | R | 1000 | M | 1 | 0 | 4 | 2 | 1 | 1 | 6 | 5 | 1 | 1 | 3 | 3 |


| Page Table |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Reference (virtual address) | Read / Writ e | Left <br> Most <br> Four Bits | Page <br> Fault | VPN 0 |  |  | VPN 1 |  |  | VPN 2 |  |  | VPN 3 |  |  | VPN 4 |  |  | VPN 5 |  |  | VPN 6 |  |  | VPN 7 |  |  |
|  |  |  |  | V | D | PPN | V | D | PPN | V | D | $\begin{aligned} & \mathrm{PP} \\ & \mathrm{~N} \\ & \hline \end{aligned}$ | V | D | $\begin{array}{\|l\|} \hline \text { PP } \\ \mathrm{N} \\ \hline \end{array}$ | V | D | PPN | V | D | PPN | V | D | $\begin{aligned} & \hline \text { PP } \\ & \mathrm{N} \\ & \hline \end{aligned}$ | V | D | PPN |
| 0xA1F4 | R | 1010 | Y | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 1 | 0 | 2 | 0 |  |  | 0 |  |  |
| 0xFEA6 | R | 1111 | Y | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 1 | 0 | 2 | 0 |  |  | 1 | 0 | 3 |
| 0xE208 | W | 1110 | N | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 1 | 0 | 2 | 0 |  |  | 1 | 0 | 3 |
| 0x2020 | R | 0010 | Y | 0 |  |  | 1 | 0 | 4 | 0 |  |  | 0 |  |  | 0 |  |  | 1 | 0 | 2 | 0 |  |  | 1 | 0 | 3 |
| 0xB03E | W | 1011 | N | 0 |  |  | 1 | 0 | 4 | 0 |  |  | 0 |  |  | 0 |  |  | 1 | 0 | 2 | 0 |  |  | 1 | 0 | 3 |
| 0xD021 | W | 1101 | Y | 0 |  |  | 1 | 0 | 4 | 0 |  |  | 0 |  |  | 0 |  |  | 1 | 0 | 2 | 1 | 0 | 5 | 1 | 1 | 3 |
| 0x689A | R | 0110 | Y | 0 |  |  | 1 | 0 | 4 | 0 |  |  | 1 | 0 | 3 | 0 |  |  | 1 | 0 | 2 | 1 | 0 | 5 | 0 |  |  |
| 0x345C | W | 0011 | N | 0 |  |  | 1 | 0 | 4 | 0 |  |  | 1 | 0 | 3 | 0 |  |  | 1 | 1 | 2 | 1 | 0 | 5 | 0 |  |  |
| 0xCFDC | W | 1100 | N | 0 |  |  | 1 | 0 | 4 | 0 |  |  | 1 | 0 | 3 | 0 |  |  | 1 | 1 | 2 | 1 | 0 | 5 | 0 |  |  |
| 0x7ED2 | W | 0111 | N | 0 |  |  | 1 | 0 | 4 | 0 |  |  | 1 | 0 | 3 | 0 |  |  | 1 | 1 | 2 | 1 | 0 | 5 | 0 |  |  |
| 0x8038 | R | 1000 | Y | 0 |  |  | 1 | 1 | 4 | 0 |  |  | 1 | 0 | 3 | 1 | 0 | 2 | 0 |  |  | 0 |  |  | 0 |  |  |

** Note: V - Valid Bit, D - Dirty Bit, VPN - Virtual Page Number, PPN - Physical Page Number.

Blank TLB

| Reference (virtual address) | Read/ Write | Left Most Four Bits | Hit/ <br> Miss | Entry 0 |  |  |  | Entry 1 |  |  |  | Entry 2 |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | V | D | VPN | PPN | V | D | VPN | PPN | V | D | VPN | PPN |
| 0xA1F4 | R |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 0xFEA6 | R |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 0xE208 | W |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 0x2020 | R |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 0xB03E | W |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 0xD021 | W |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 0x689A | R |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 0x345C | W |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 0xCFDC | W |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 0x7ED2 | W |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 0x8038 | R |  |  |  |  |  |  |  |  |  |  |  |  |  |  |


| Blank Page Table |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Reference (virtual address) | Read / Writ e | Left <br> Most <br> Four Bits | Page <br> Fault | VPN 0 |  |  | VPN 1 |  |  | VPN 2 |  |  | VPN 3 |  |  | VPN 4 |  |  | VPN 5 |  |  | VPN 6 |  |  | VPN 7 |  |  |
|  |  |  |  | V | D | PPN | V | D | PPN | V | D | $\begin{aligned} & \mathrm{PP} \\ & \mathrm{~N} \end{aligned}$ | V | D | $\begin{array}{\|c} \mathrm{PP} \\ \mathrm{~N} \\ \hline \end{array}$ | V | D | PPN | V | D | PPN | V | D | $\begin{array}{\|l\|} \hline \mathrm{PP} \\ \mathrm{~N} \\ \hline \end{array}$ | V | D | PPN |
| 0xA1F4 | R |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 0xFEA6 | R |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 0xE208 | W |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 0x2020 | R |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 0xB03E | W |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 0xD021 | W |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 0x689A | R |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 0x345C | W |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 0xCFDC | W |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 0x7ED2 | W |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 0x8038 | R |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

** Note: V - Valid Bit, D - Dirty Bit, VPN - Virtual Page Number, PPN - Physical Page Number.

## Question 3

The virtual page number can be broken up into two pieces, a "page table number" and a "page table offset." The page table number can be used to index a first-level page table that provides a physical address for a second-level page table, assuming it resides in memory (if not, a first-level page fault will occur and the page table itself will need to be brought in from disk). The page table off- set is used to index into the second-level page table to retrieve the physical page number. One obvious way to arrange such a scheme is to have the second-level page tables occupy exactly one page of memory. Assuming a 32-bit virtual address space with 4 KB pages and 4 bytes per page table entry, how many bytes will each program need to use to store the first-level page table (which must always be in memory)? Provide figures similar to Figures 7.20, 7.21, and 7.22 that demonstrate your understanding of this idea.

## Answer

Using a 32-bit virtual address and 4 KB page size, the virtual address is par- titioned into a 20-bit virtual page number and a 12 -bit page offset. We divide the virtual page number into two 10-bit fields. The first field is the page table number and is used as an index into the first-level page table. The size of the first-levelpage table in $2^{10}$ entries $\times 4$ bytes/entry $=2^{12}$ bytes = one page.

## Question 4

Assuming that we use the two-level hierarchical page table described in Question 3 and that exactly one second-level page table is in memory and exactlyhalf of its entries are valid, how many bytes of memory in our virtual address space actually reside in physical memory? (Hint: The second-level page table occupies exactly one page of physical memory.)

## Answer

Pages are 4-KB in size and each entry uses 32 bits, so we get 1 K worth of page table entries in a page. Each of these entries points to a physical 4-KB page, making it possible to address $2^{10} \times 2^{12}=2^{22}$ bytes $=4 \mathrm{MB}$ of memory. But only half of these are valid, so 2 MB of our virtual address space would be in physical memory. If there are 1 K worth of entries per page table, the page table offset will occupy 10 bits and the page table number also 10 bits. Thus, we only need 4 KB to store the first- levelpage table as well.


[^0]:    ** Note: VPN - Virtual Page Number, PPN - Physical Page Number.

