Quiz (Lecture 2)

Q1: Indicate if each of the following statements is true (T) or false (F) (2.5 points):

Accessing a fully associative cache is slower than a direct map cache of the same size  
Larger cache blocks leads to a smaller miss penalty  
The number of blocks in the cache determine the block size  
A write back policy means that each write to the cache is also written back to memory  
The dirty bit is used to indicate that a block in cache does not contain valid data

Q2: Complete the following sentences (4 points):

Assuming an 8-word, direct mapped, cache with block size = 1 word:
Memory word address 19 is cached in index 3 (in decimal) and its tag is 2 (in decimal)
Memory word address 001100011 is cached in index 011 (in binary) and its tag is 001100 (in binary)

Assuming a 32-word, direct mapped, cache with block size = 4 word:
Memory word address 19 is cached in block index 4 (in decimal) and its tag is 0 (in decimal)
Memory word address 001100011 is cached in block index 000 (binary) and its tag is 0011 (binary)

Q3: In a 32-bits architecture where a byte address is given by 32 bits b31, b30, ... , b1, b0, identify the bits that are used for the tag if the cache size is 8Kbyte and the cache block size = 4 words (16 bytes) (1.5 points).

The tag bits are: b31 , b30 , .... , b14 , b13

b31 b30 b29 ... b2 b1 b0