**State Elements**

RS latch
- R, S control mode (reset, set, storage)
- Q, Q' track R and S
- R=1, S=1 invalid

D flip-flop (falling or negative edge triggered)
- Two cascaded D latches
- C=1 means 1st latch transparent, 2nd latched
- C=0 means 1st latch latched, 2nd transparent
- Output changes on falling edge (C: 1 => 0)

D latch
- C controls mode (0 = latched, 1 = transparent)
- D is data input ("copied" during transparent)
- Signal value triggered: Q, Q' track D when C=1
- Guarantees R=1, S=1 can not be done

D flip-flop (rising or positive edge triggered)
- Same as falling edge triggered
- Output changes on rising edge (C: 0 => 1)

**Signaling Behavior**

Q goes high when R=0, S=1

Storage mode

Q goes low when R=1, S=0
Signaling Behavior

**D latch behavior**
- Q goes C=1, D=1
- Q tracked D when C=1
- Q went low C=1, D=0
- Q stays low b/c C=0

**D flip-flop (falling edge triggered)**
- no change b/c not a falling edge
- tracks D at time of falling edge
- no change b/c not falling edge
**Signaling Behavior**

- **RS latch behavior**
- **D latch behavior**
- **D flip-flop (falling edge triggered)**

**Example circuits and clocking**

- Suppose we want to:
  - 1-bit value A stored in a D flip-flop
  - 1-bit value B stored in a D flip-flop
  - 1-bit value C stored in a D flip-flop
  - Do addition of A and B, producing C

- C = A + B
  - What is the circuit?
  - Need three D flip-flops
  - Need one 1 bit adder
Example circuits and clocking

- Is there any difference in the delay with this one?

- In fact, sequential logic often looks like this....
Example circuits and clocking

- Now, suppose we want to build a 4-bit counter?
  - Counter increments by 1 for a clock pulse (falling edge event)
  - 4 1-bit adders
  - 4 1-bit D flip-flops

- What’s the circuit?
- How often to “pulse” the clock (increment counter)?

Recall: The flip-flops are edge triggered -- assuming falling edge (negative)

How often can an edge event happen?

No more frequent than the maximum propagation delay
Let’s compute the delay -- assume 2ns for latch to stabilize and 4ns for adder
Example circuits and clocking

- Values of output bits **must all be stable**
  - I.e., can’t pulse the clock (increment) until all four bits are computed

- Adder circuit is ripple-carry: Must wait for carries
  - 4ns per adder
  - 4-bit adder
  - thus, $4 \times 4\text{ns} = 16\text{ns}$ for the adder

- Flip-flops
  - Must wait for 1\text{st} latch of last bit to stabilize (others done in parallel)
  - Must wait for 2\text{nd} latch of all bits to stabilize (all done in parallel)
  - thus, $2\text{ns} + 2\text{ns} = 4\text{ns}$

- Overall delay = $16\text{ns} + 4\text{ns} = 20\text{ns}$. Clock pulse is 20ns.

Example circuits and clocking

Clock pulse is 20ns
Flip-flops are falling edge triggered
Thus, a clock falling edge every 20ns
Example circuits and clocking

Can we build a counter with just flip-flops?

What's the maximum clock pulse rate?