

Creating a Single Datapath

- **Data path segments for**
 - **Fetch**
 - **Execution**
 - **Arithmetic operations** (R-type instructions)
 - Register file (read), ALU, register file (write)
 - **Load/store**
 - Register file (read), ALU (effective address), data memory (read/write), register file (write on load)
 - **Branches**
 - Register file (read), ALU (comparison), Adder (branch target address), PC (update)
- **Can we combine these segments so they are shared?**

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Creating a Single Datapath

- **Yes!**
- **A simple datapath**
 - **Execute instructions in a single cycle**
 - **Hence, no datapath element used more than once by an instruction in a single cycle**
 - Any element needed more than once: must be duplicated
 - **Share datapath elements among different instruction classes**

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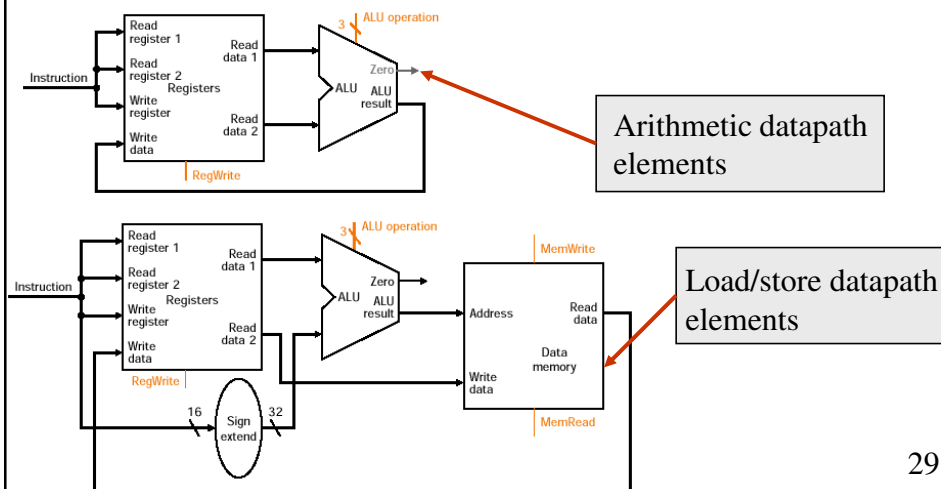
Sharing Datapath Elements

- Share datapath element among instruction classes
 - E.g., ALU between arithmetic, branch, load/store

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Sharing Datapath Elements

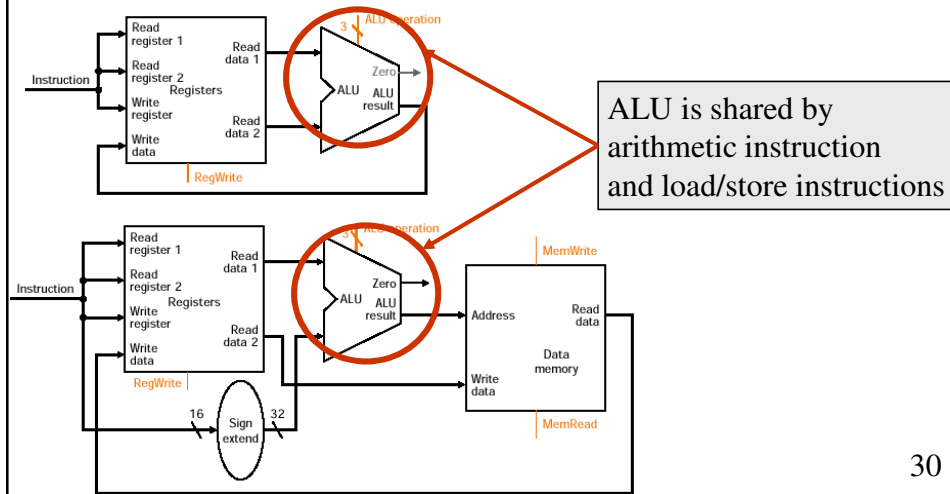
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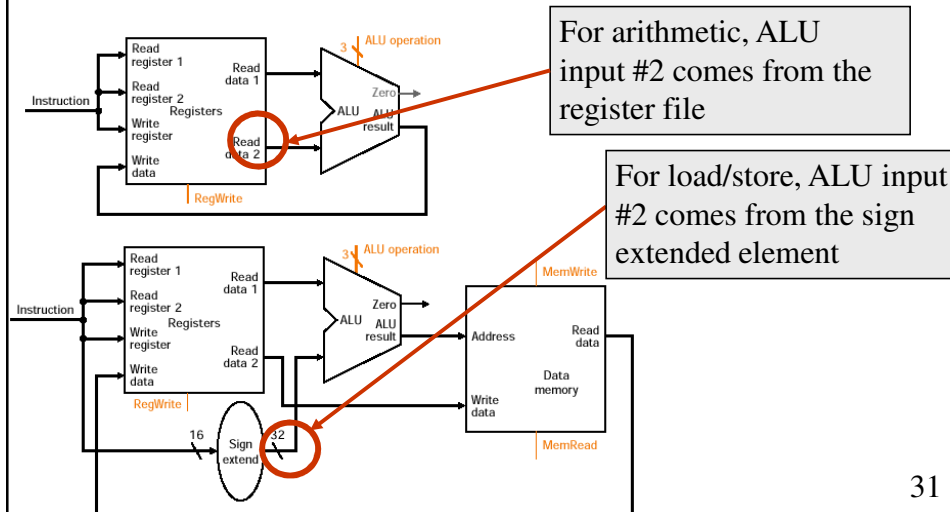
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Sharing Datapath Elements

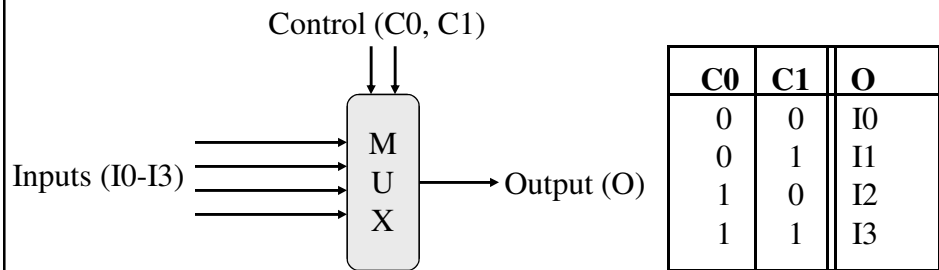
- Sharing may need to - wire inputs to multiple sources
 - Pick among possible input sources



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Selecting Among Inputs

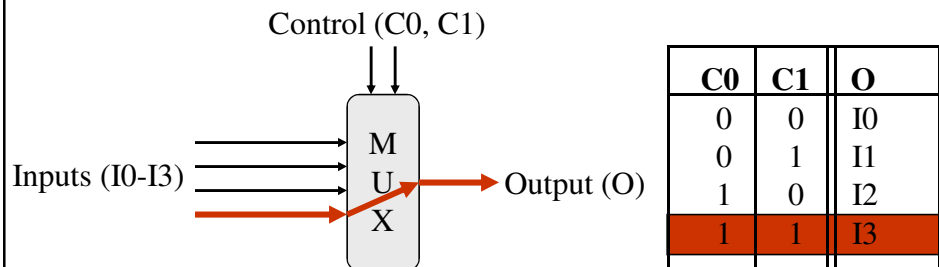
- To select among inputs - use a **multiplexor**
- Multiplexor
 - Several inputs
 - One output
 - Control lines to select among different inputs



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Selecting Among Inputs

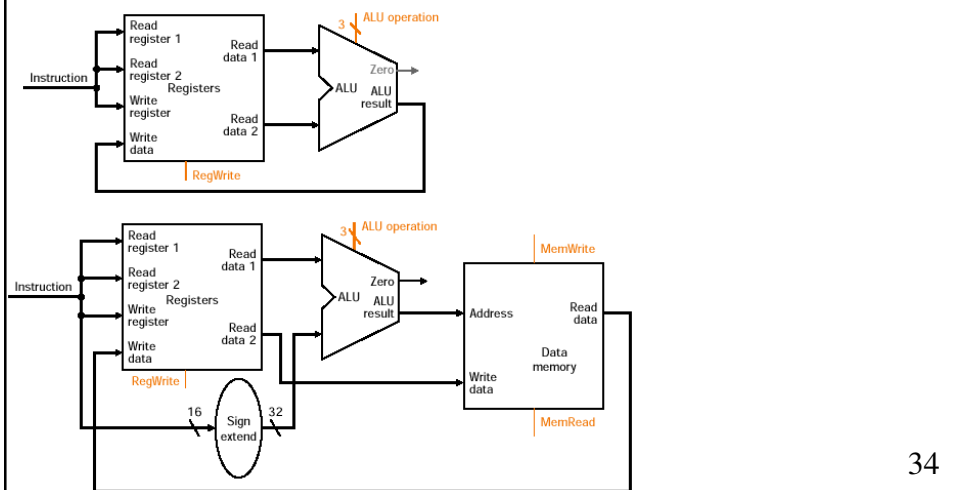
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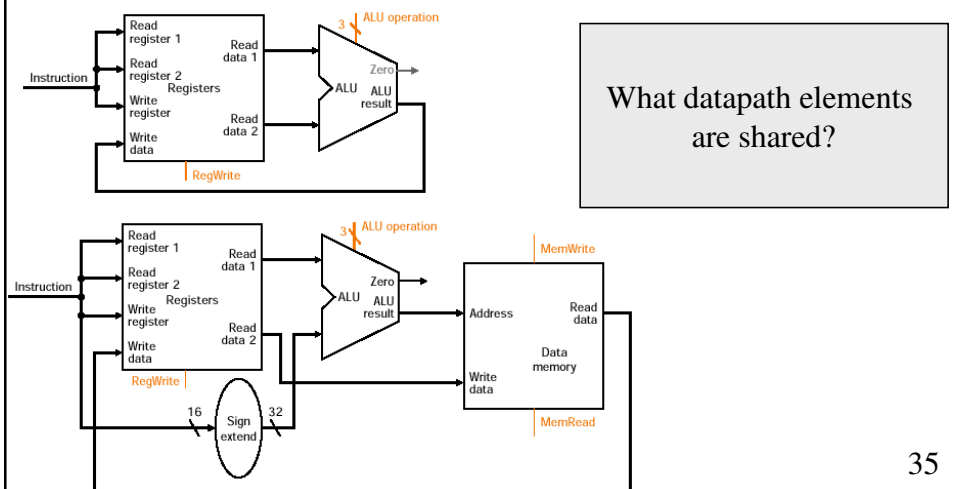
Composing Datapaths

- Let's compose the arithmetic instruction datapath with the load/store (memory) instruction datapath



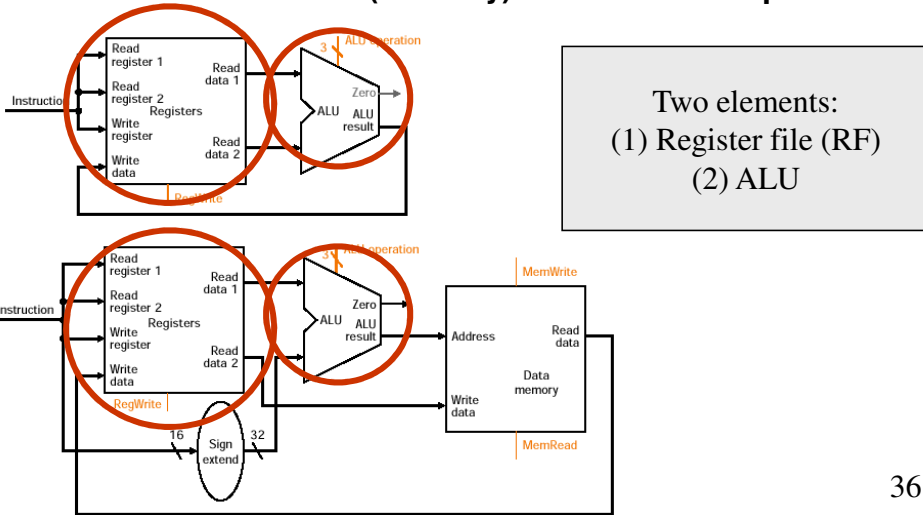
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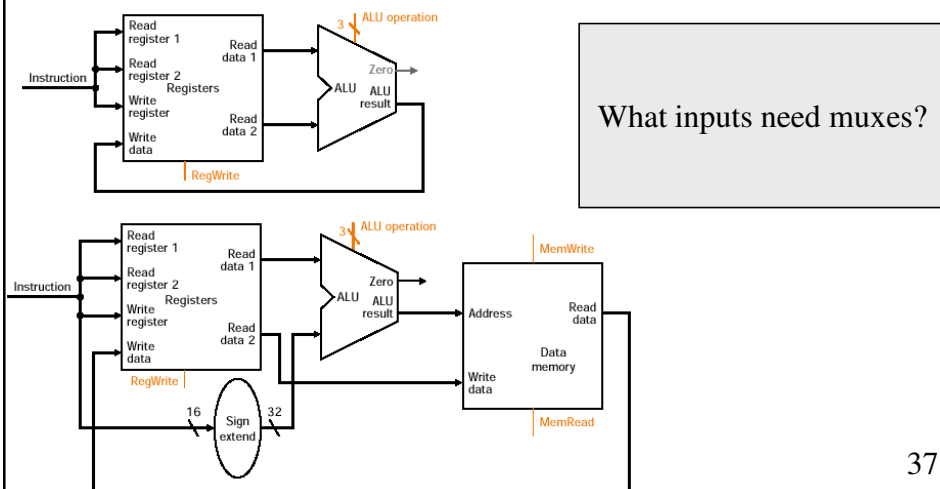
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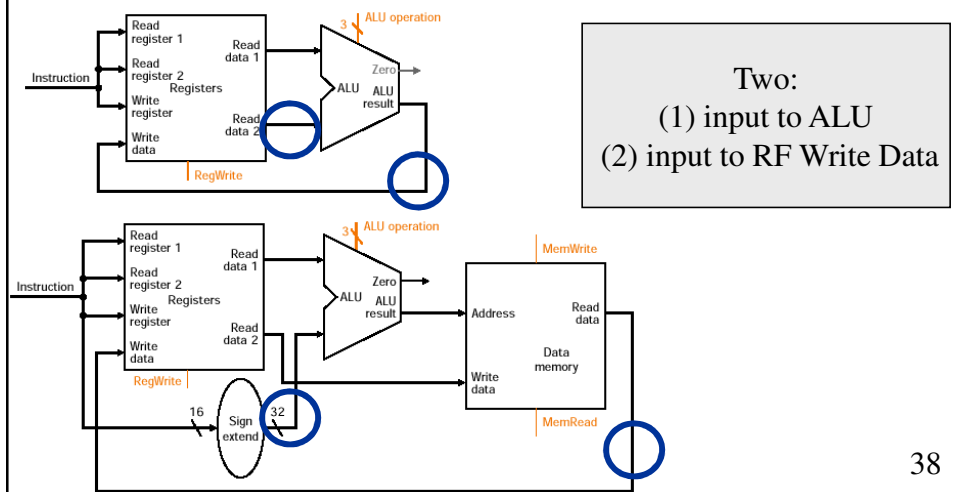
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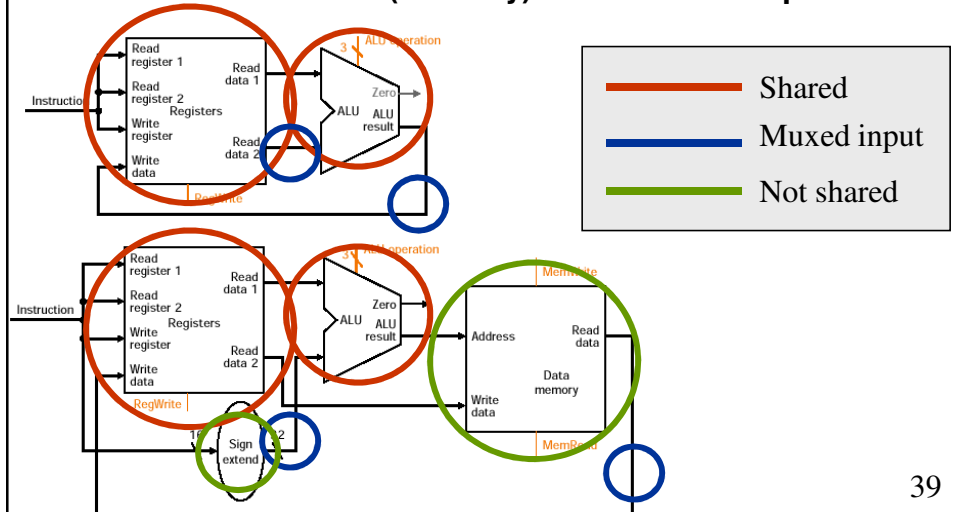
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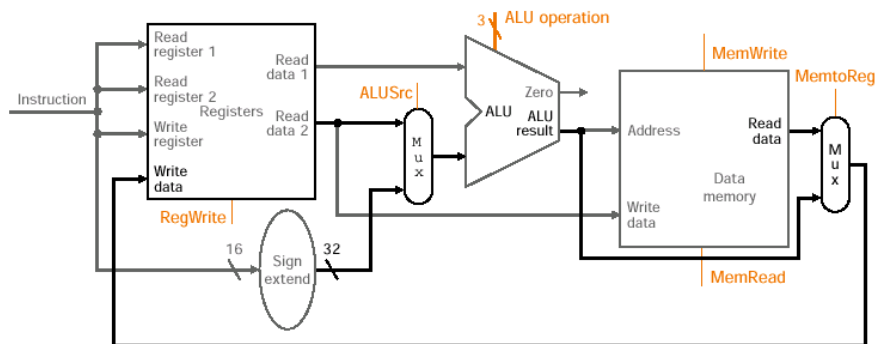
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Composed Arithmetic and L/S Datapath

- Two muxes -
 - 1. select among register or sign-extend
 - 2. select input to RF from ALU or data memory
- Need control signals for muxes, ALU, RF, Memory

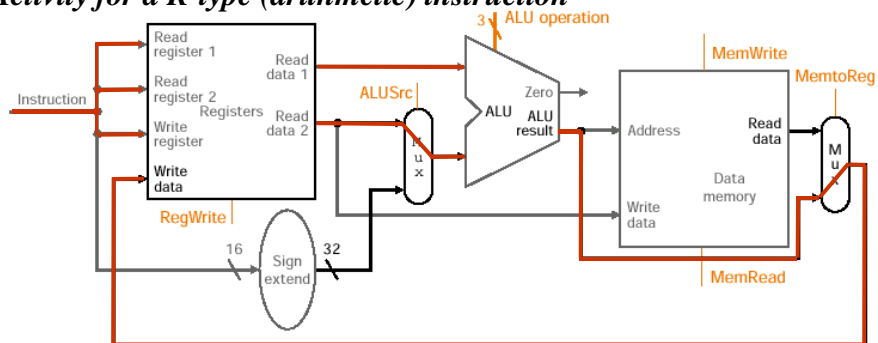


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Activity for a R-type (arithmetic) instruction

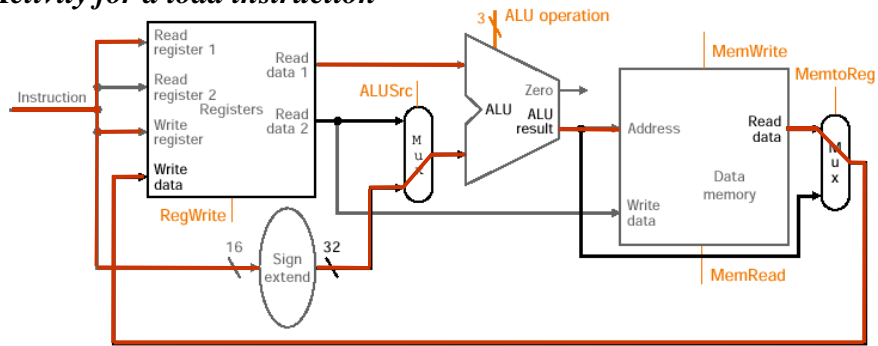


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Activity for a load instruction

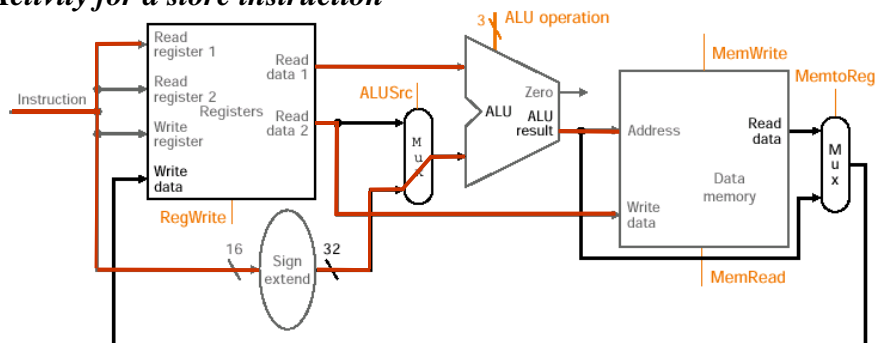


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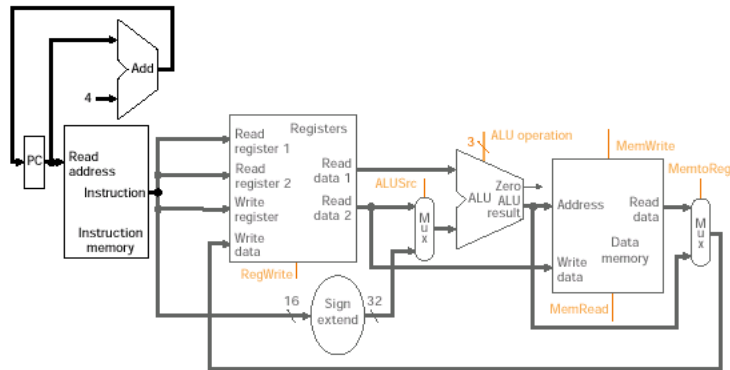
Activity for a store instruction



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Datapath with Fetch

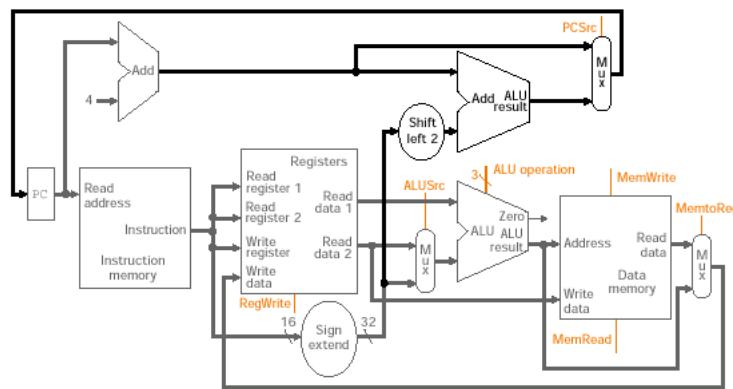
- Composed fetch with arithmetic and load/store datapath
- Separate adder for PC increment



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Datapath with Branches

- Separate ALU for computing branch target
- Shifter (by 2) for 16-bit offset constant
- Mux to select among next address (PC+4) or target address from branch ALU



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