

## Setting Control Signals

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- All signals except PCSrc set based on opcode
- PCSrc set using opcode and zero output from ALU
  - PCSrc = (Opcode == beq AND zero == true)
  - Branch is control for Opcode == Beq

	<u>R-format</u>	<u>lw</u>	<u>sw</u>	<u>beq</u>
RegDst	1	0	X	X
ALUSrc	0	1	1	0
MemToReg	0	1	X	X
RegWrite	1	1	0	0
MemRead	0	1	0	0
MemWrite	0	0	1	0
Branch	0	0	0	1
ALUOp	10	00	00	01